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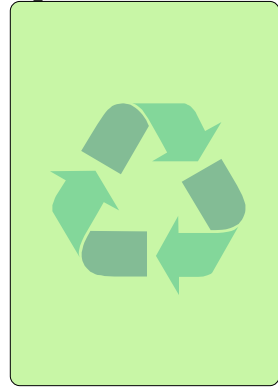
C

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U_DB_Common
DB_Common



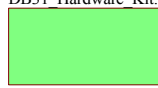
U_PSU
PSU.SCHDOC




U_Bypass_Board
DB_Bypass



U_DB31_Hardware_Kit
DB31_Hardware_Kit.SchDoc



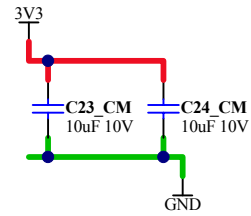
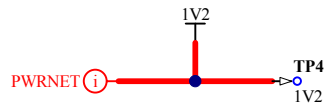
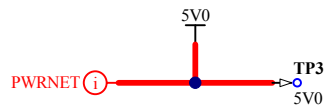
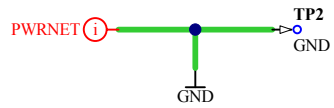
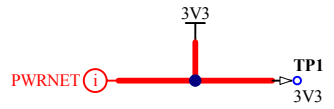
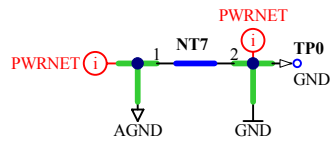
Sheet Title DB31 Top Level			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005	Revision:07		
Date: 2/12/2008	Time: 1:17:14 PM	Sheet 1 of 21		
File: DB31_Top.SchDoc				

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Shared Bypass Caps

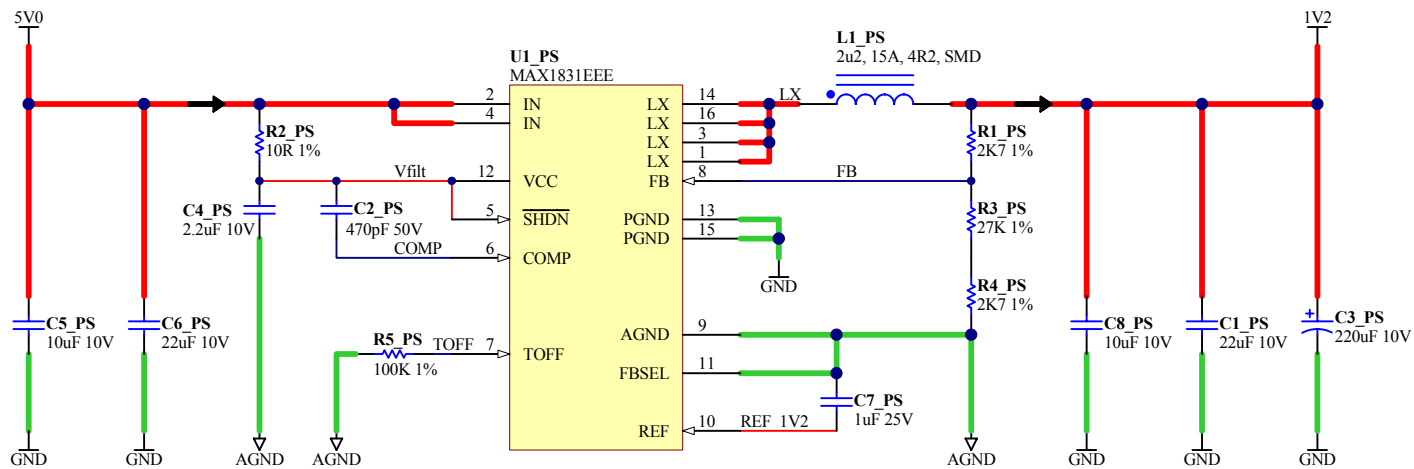
U_PSU_MAX1831_1V2_ALT
PSU_MAX1831_1V2_ALT



Sheet Title Power Supplies		
Project Title DB31 - Daughter Board Cyclone2		
Size: A4	Assy: D-820-0005	Revision:07
Date: 2/12/2008	Time: 1:17:14 PM	Sheet 2 of 21
File: PSU.SCHDOC		

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 Australia





Sheet Title **Power Supply MAX1831 (1V2)**

Project Title **DB31 - Daughter Board Cyclone2**

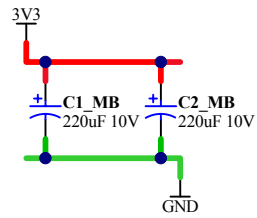
Size: A4 Assy: D-820-0005 Revision:07

Date: 2/12/2008 Time: 1:17:14 PM Sheet 3 of 21


File: PSU_MAX1831_1V2_ALT.SchDoc

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 Frenchs Forest
 NSW 2086
 Australia



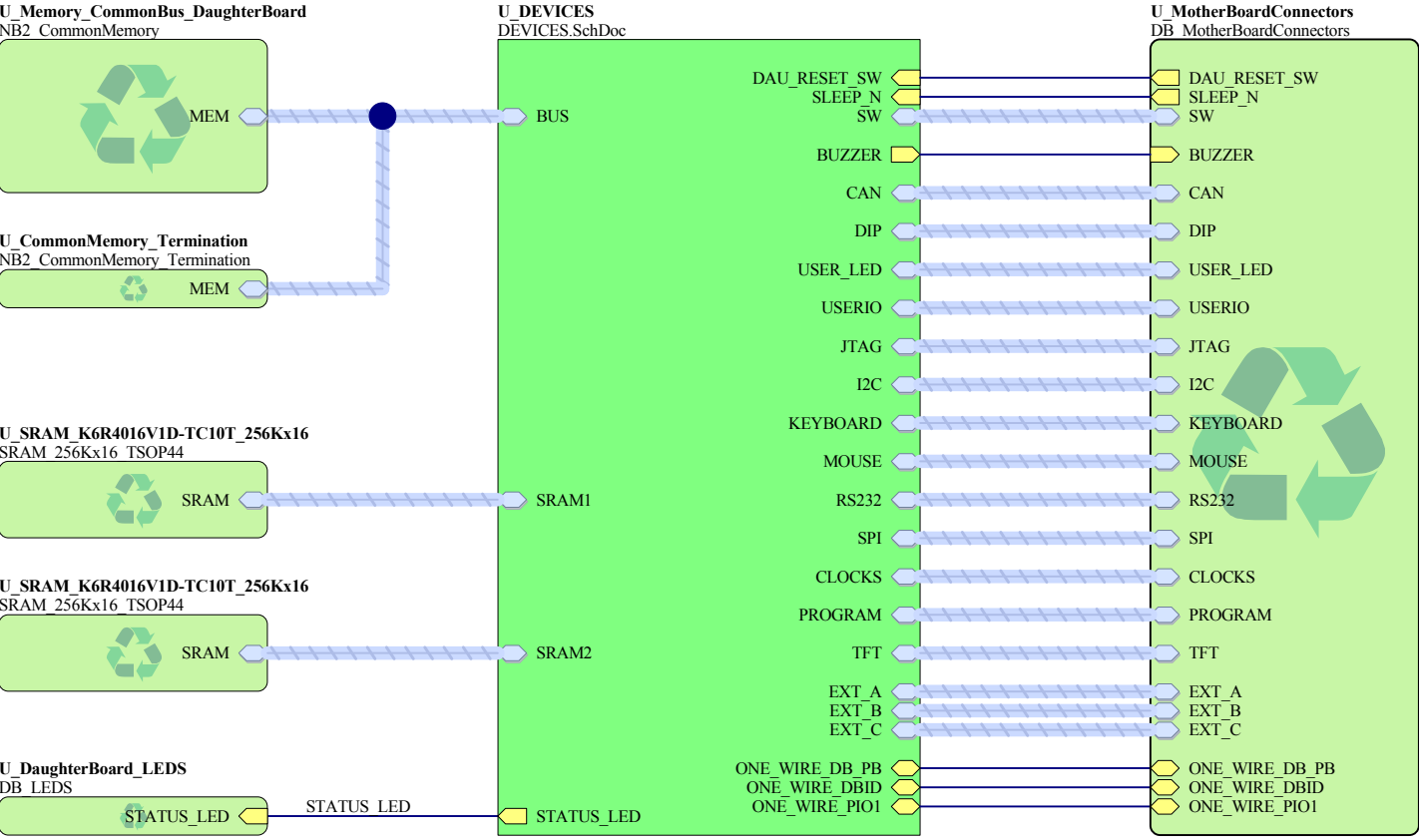


△ These decoupling capacitors are intended to assist the voltage rails on the PCB - where the decoupling capacitors for the FPGA are not close.

Sheet Title Board Bypass Capacitors		<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005			Revision:07
Date: 2/12/2008	Time: 1:17:14 PM			Sheet 4 of 21
File: DB Bypass.SchDoc				

**Top Level Schematic For Daughter Board Design
Both FPGA-Only and FPGA + MCU**

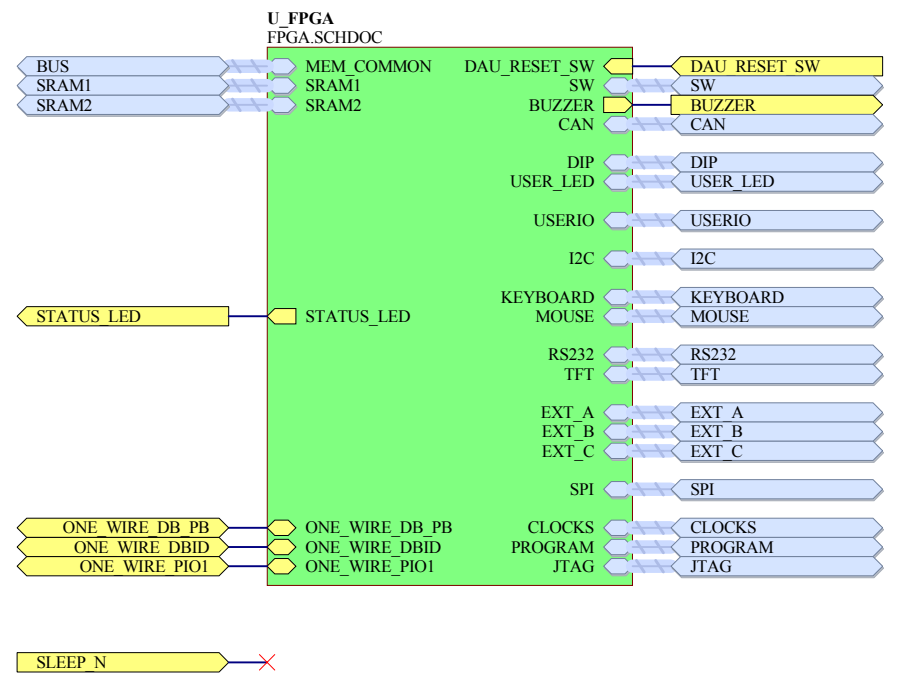
**This Device Sheet is the same for all designs.
It relies on being instantiated in a project that contains a device-specific sheet named DEVICES.SchDoc .**



Sheet Title Daughter Board Top Level		
Project Title DB31 - Daughter Board Cyclone2		
Size: A4	Assy: D-820-0005	Revision:07
Date: 2/12/2008	Time: 1:17:14 PM	Sheet 5 of 21
File: DB_Common.SchDoc		

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NSW 2086
Australia




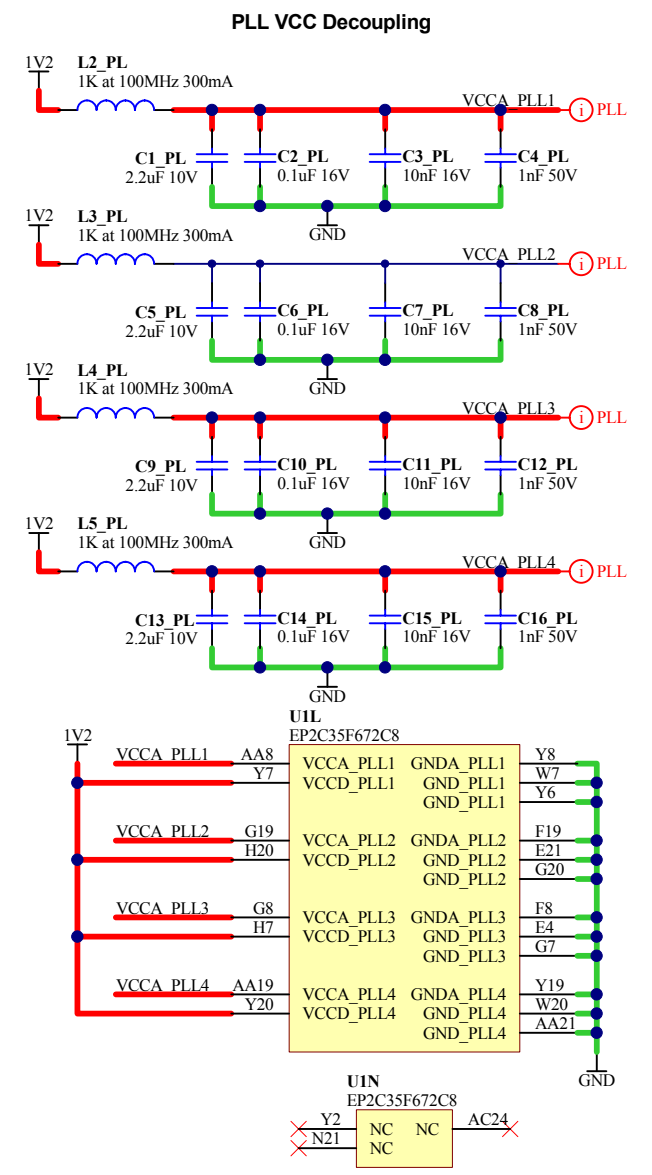
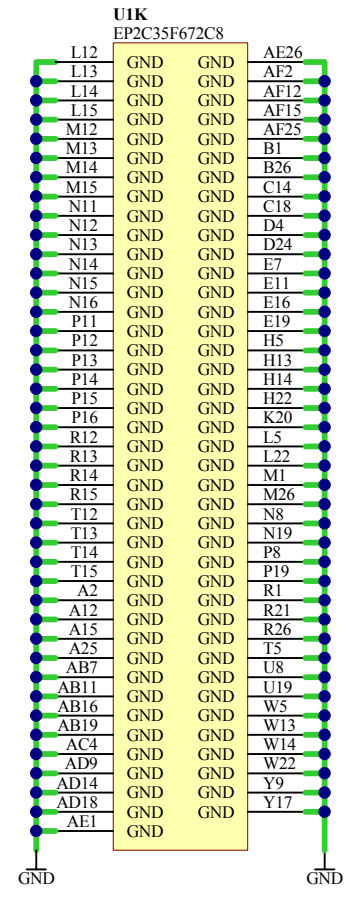
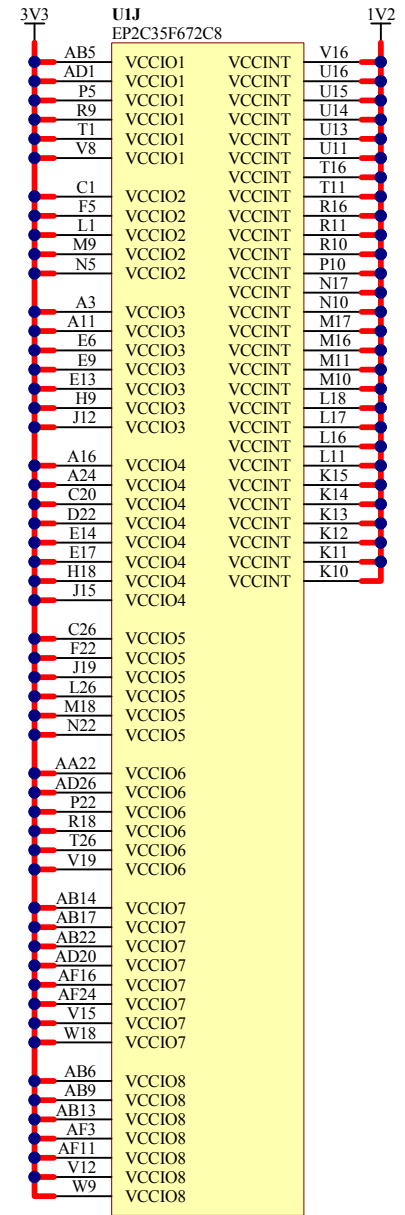
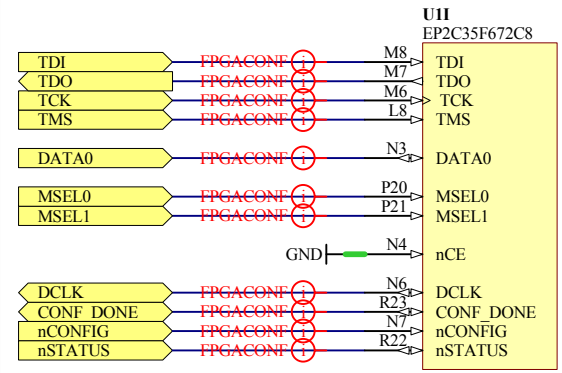


Device Specific Section of Daughter Board Design

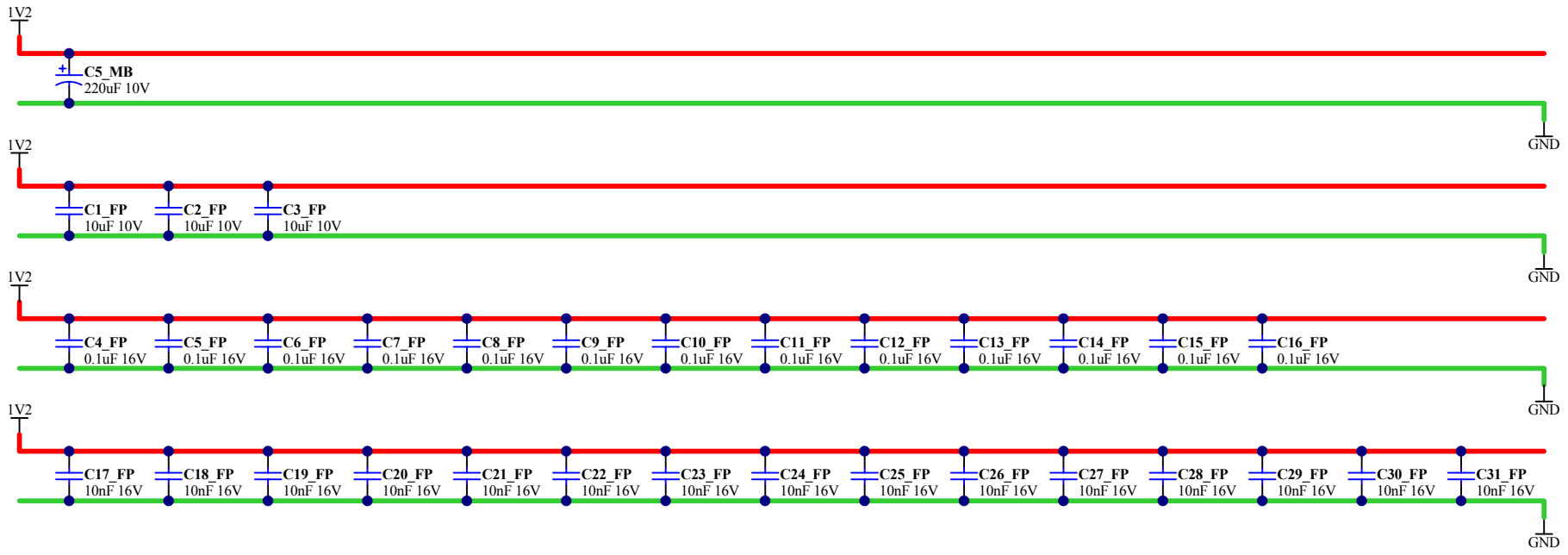
This schematic sheet (plus any child sheets) will contain the device specific parts of any daughter board designs.


This will include any FPGA or MCU devices as well as dedicated power supplies, connectors etc.

Sheet Title FPGA, LEDs and SRAM Memory		<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005			Revision:07
Date: 2/12/2008	Time: 1:17:14 PM			Sheet 6 of 21
File: DEVICES.SchDoc				



Sheet Title FPGA Power and Programming			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005	Revision: 07		
Date: 2/12/2008	Time: 1:17:14 PM	Sheet 8 of 21		
File: FPGA_NonIO.SchDoc				



Sheet Title FPGA Bypass Capacitors for 1V2		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2			
Size: A4	Assy: D-820-0005	Revision:07	
Date: 2/12/2008	Time: 1:17:14 PM	Sheet 9 of 21	
File: Bypass FPGA 1V2.SCHDOC			

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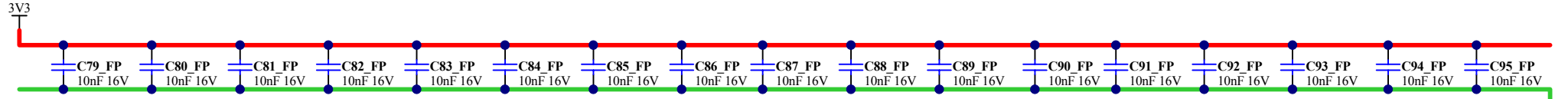
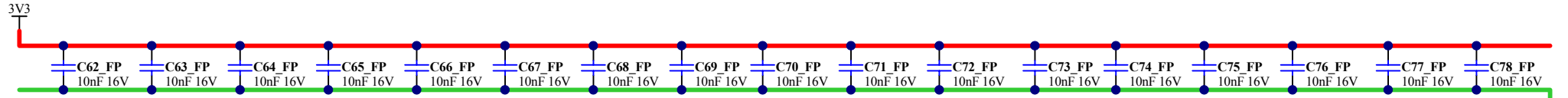
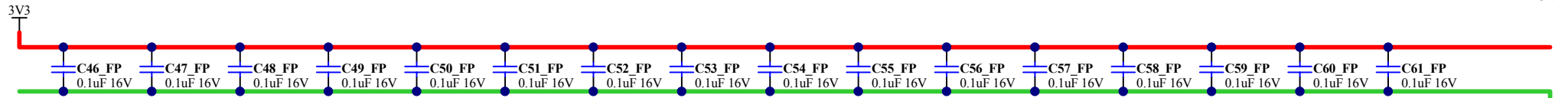
D


1

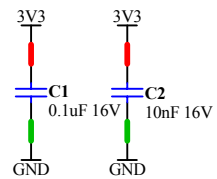
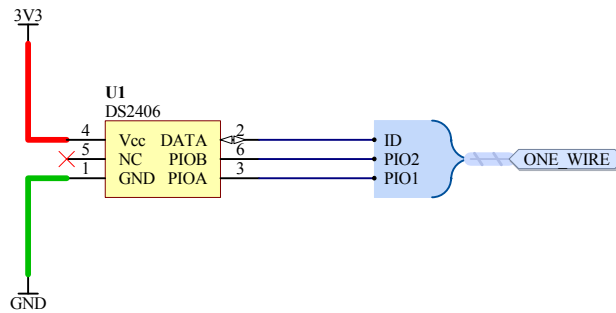
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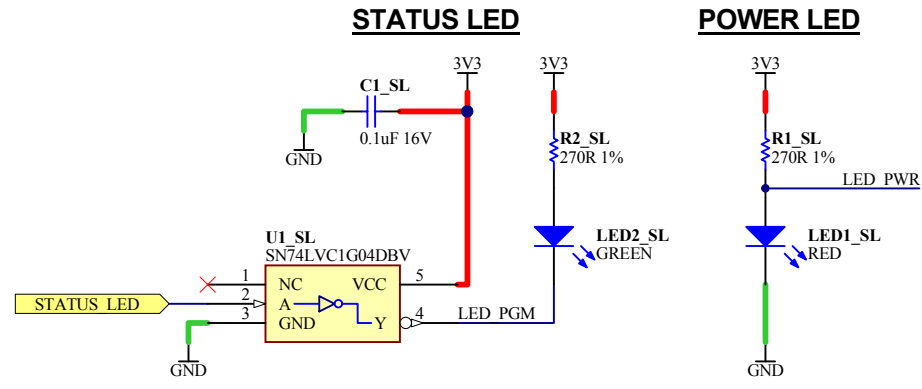
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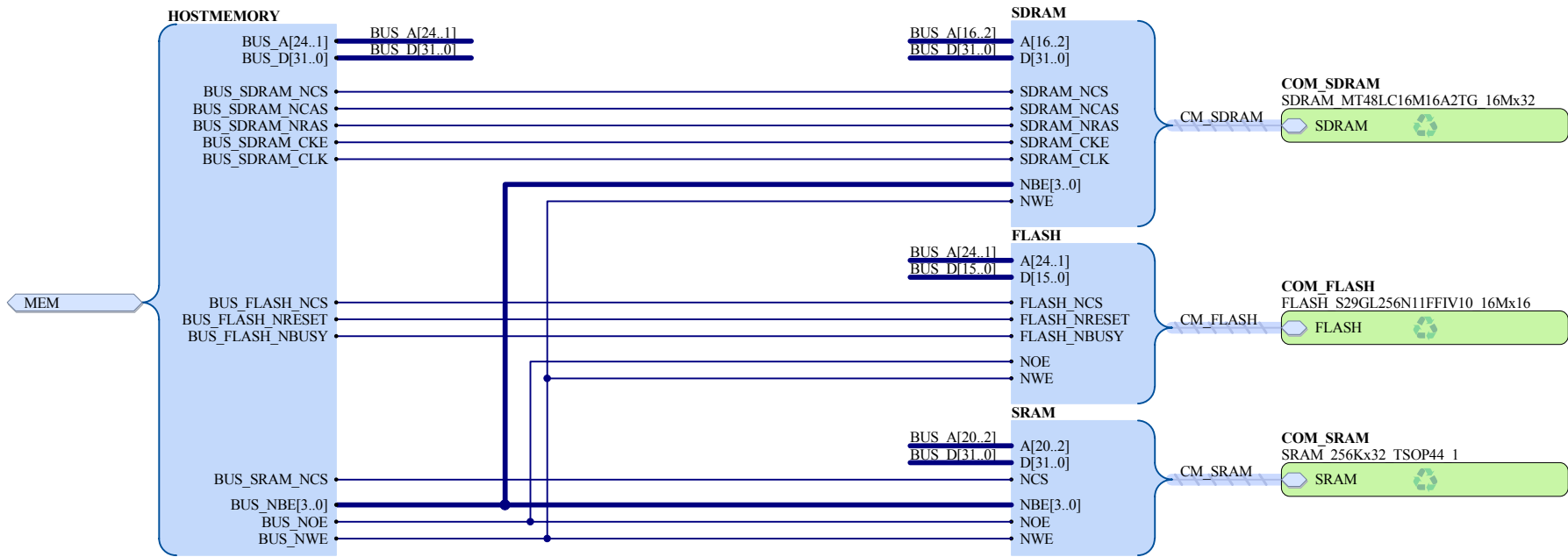
Sheet Title FPGA Bypass Capacitors for 3V3			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005	Revision: 07		
Date: 2/12/2008	Time: 1:17:14 PM	Sheet 10 of 21		
File: Bypass FPGA 3V3.SchDoc				



Sheet Title <i>1-Wire Bus ID</i>		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title <i>DB31 - Daughter Board Cyclone2</i>				
Size: A4	Assy: D-820-0005			Revision:07
Date: 2/12/2008	Time: 1:17:15 PM			Sheet 11 of 21
File: 1WB_DS2406_EPROM.SchDoc				

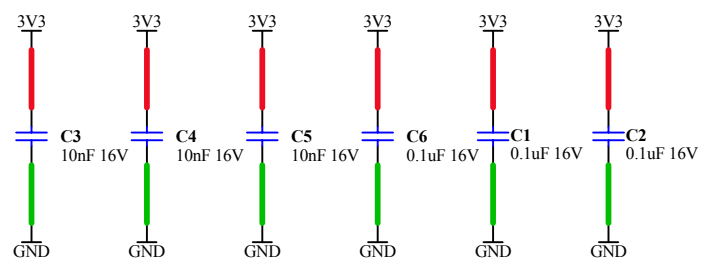
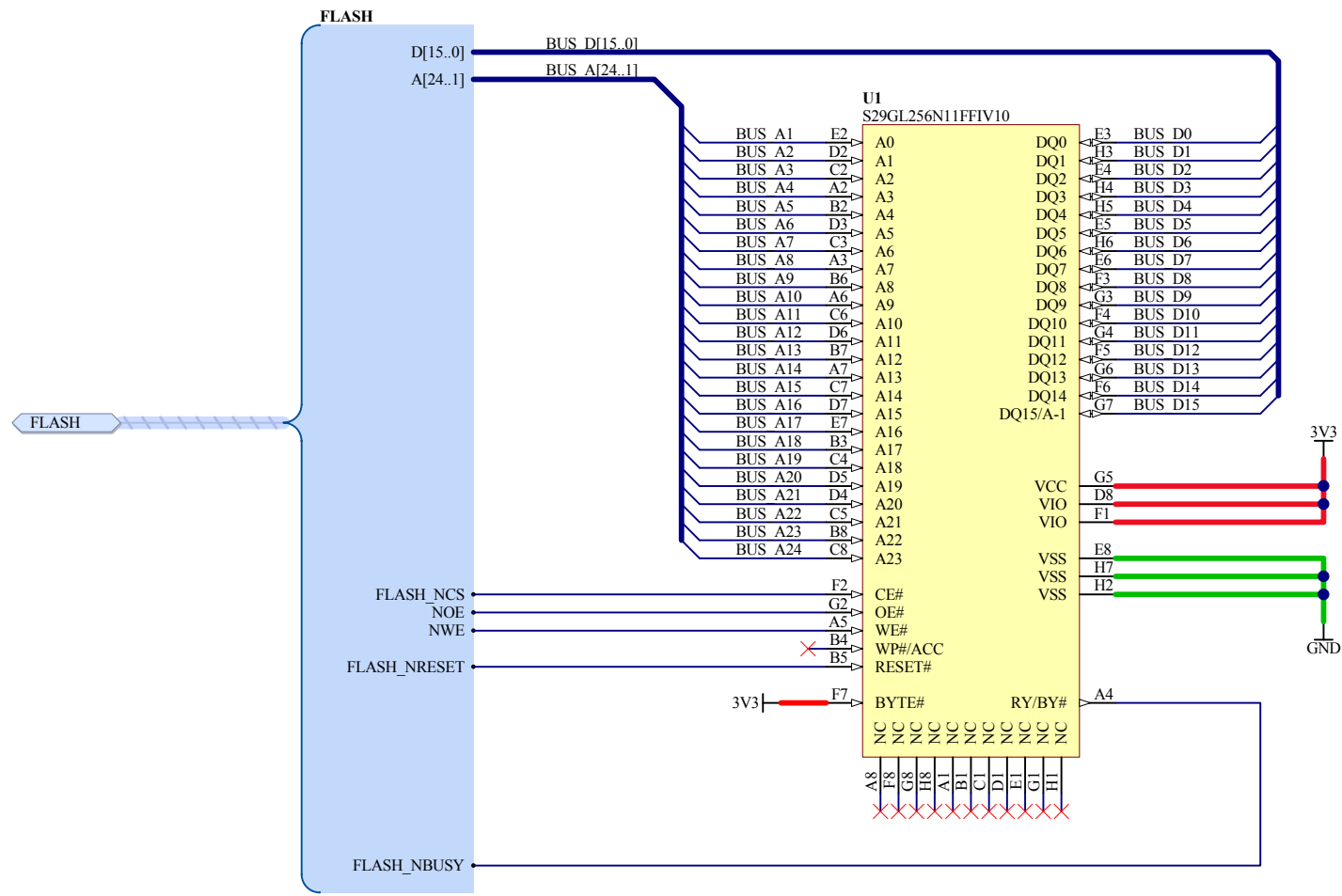


Sheet Title Daughter Board LEDs		<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005			Revision:07
Date: 2/12/2008	Time: 1:17:15 PM			Sheet 12 of 21
File: DB_LEDS.SchDoc				

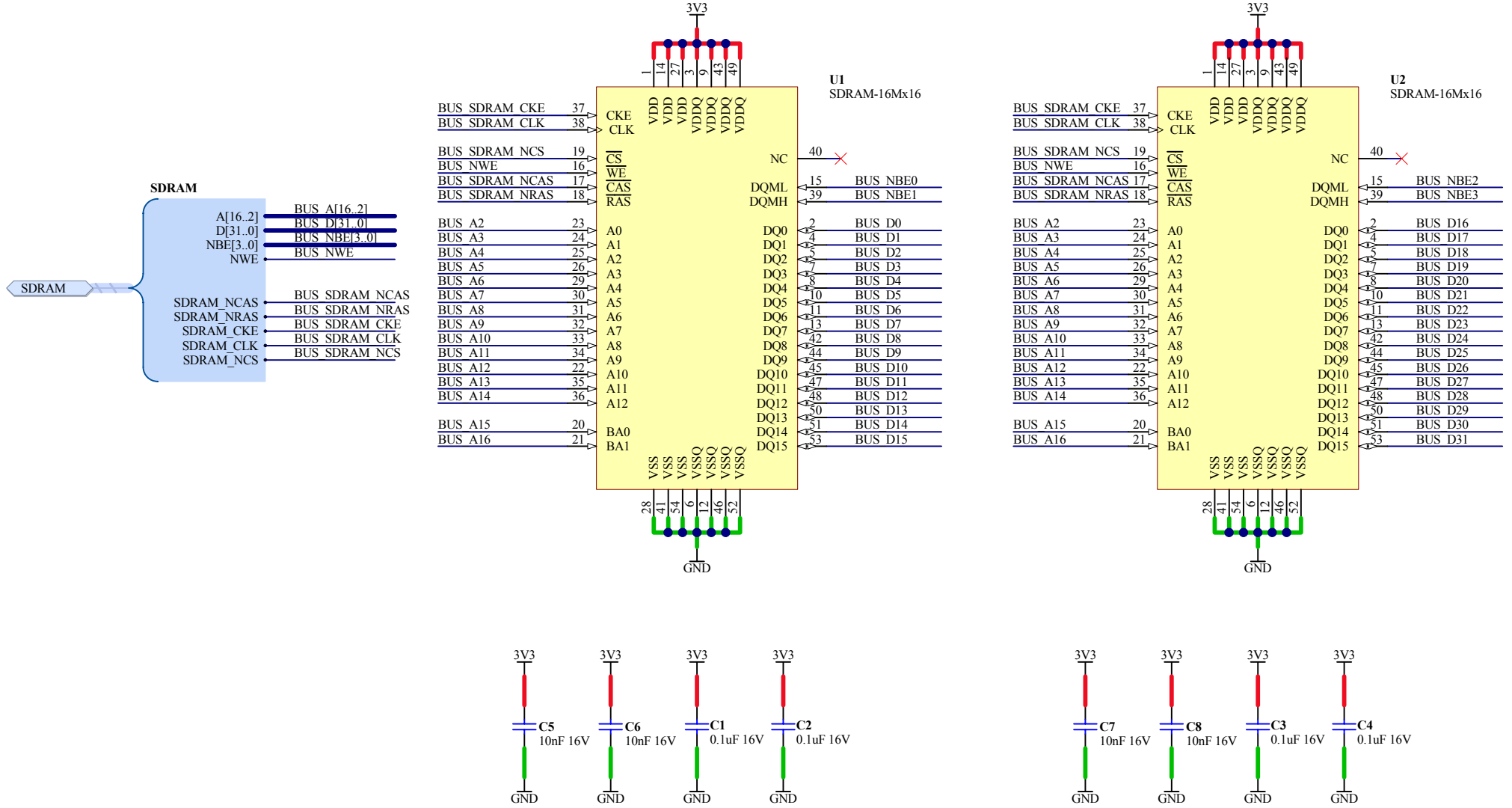


Common-Bus Memory Block
256K x 32-bit SRAM (1 MByte)
16M x 32-Bit SDRAM (64 MByte)
16M x 16-Bit Flash (32 MByte)

Sheet Title Common-Bus Memory Block			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005	Revision: 07		
Date: 2/12/2008	Time: 1:17:15 PM	Sheet 13 of 21		
File: NB2_CommonMemory.SchDoc				

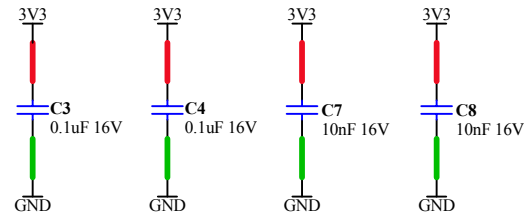
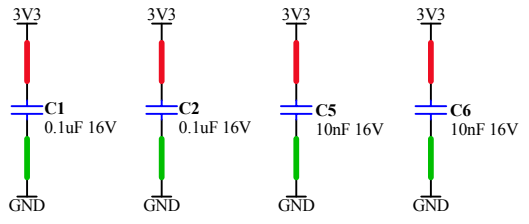
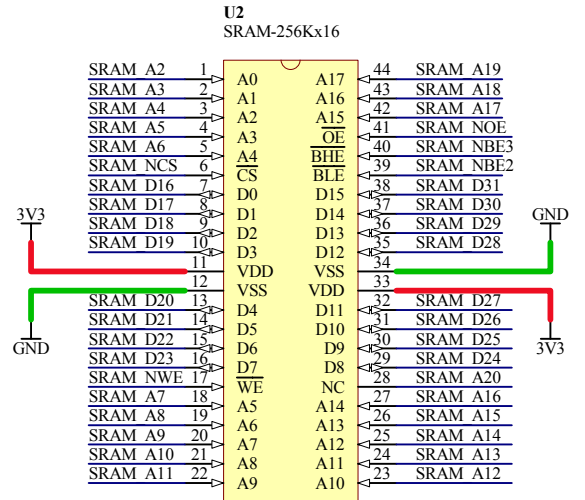
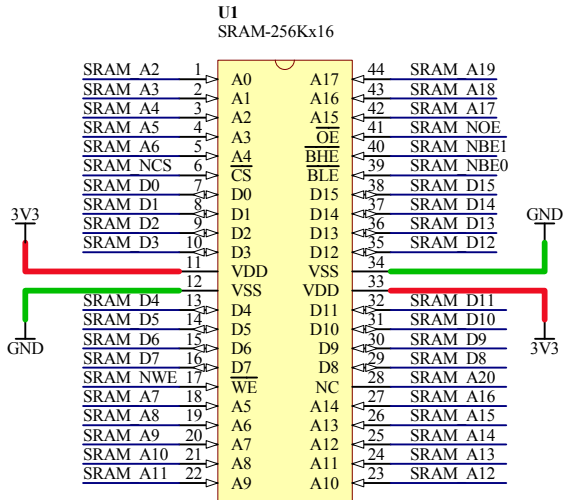
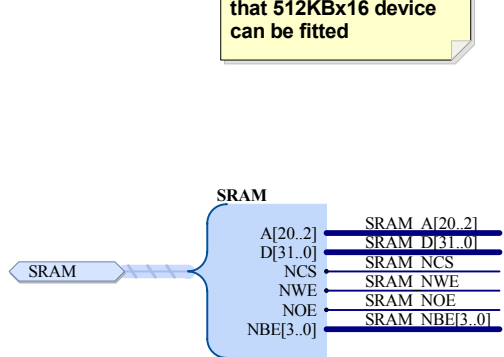


Sheet Title 16M x 16 Flash Memory (BGA)			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005	Revision: 07		
Date: 2/12/2008	Time: 1:17:15 PM	Sheet 14 of 21		
File: FLASH_S29GL256N11FFIV10_16Mx16.SchDoc				

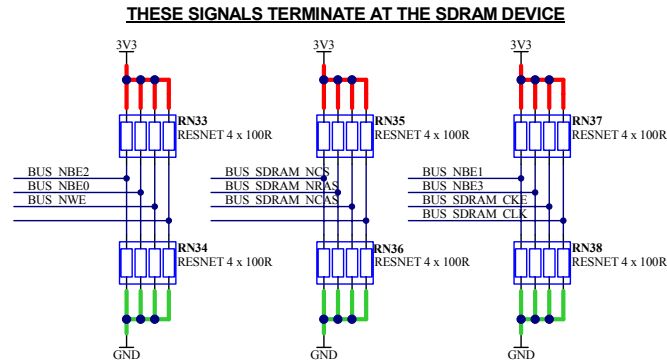
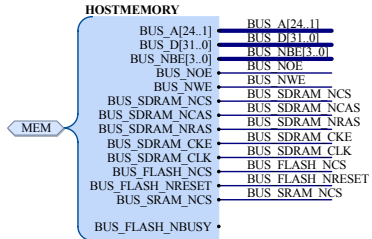


Sheet Title 16M x 32 SDRAM TSOP54 x 2			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005	Revision: 07		
Date: 2/12/2008	Time: 1:17:15 PM	Sheet 15 of 21		
File: SDRAM_MT48LC16M16A2TG_16Mx32.SchDoc				

A18 is connected so that 512KBx16 device can be fitted



Sheet Title 256K x 32 SRAM - TSOP44 x 2		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2			
Size: A4	Assy: D-820-0005	Revision: 07	
Date: 2/12/2008	Time: 1:17:15 PM	Sheet 16 of 21	
File: SRAM 256Kx32 TSOP44 1.SchDoc			



All devices using controlled impedance outputs from the source (ie. FPGA) should use 50 ohm (2 parallel 100 ohm resistors) termination.

The Flash should be located closest to the source (FPGA).

The SRAM should be located next furthest from the source (FPGA).

The SDRAM should be located next furthest from the source (FPGA).

Terminations are to be located at the furthest distance from the source (FPGA).

Note that pins 5,6,7 and 8 of the following resnet "groups" are pin-swappable within that "group":

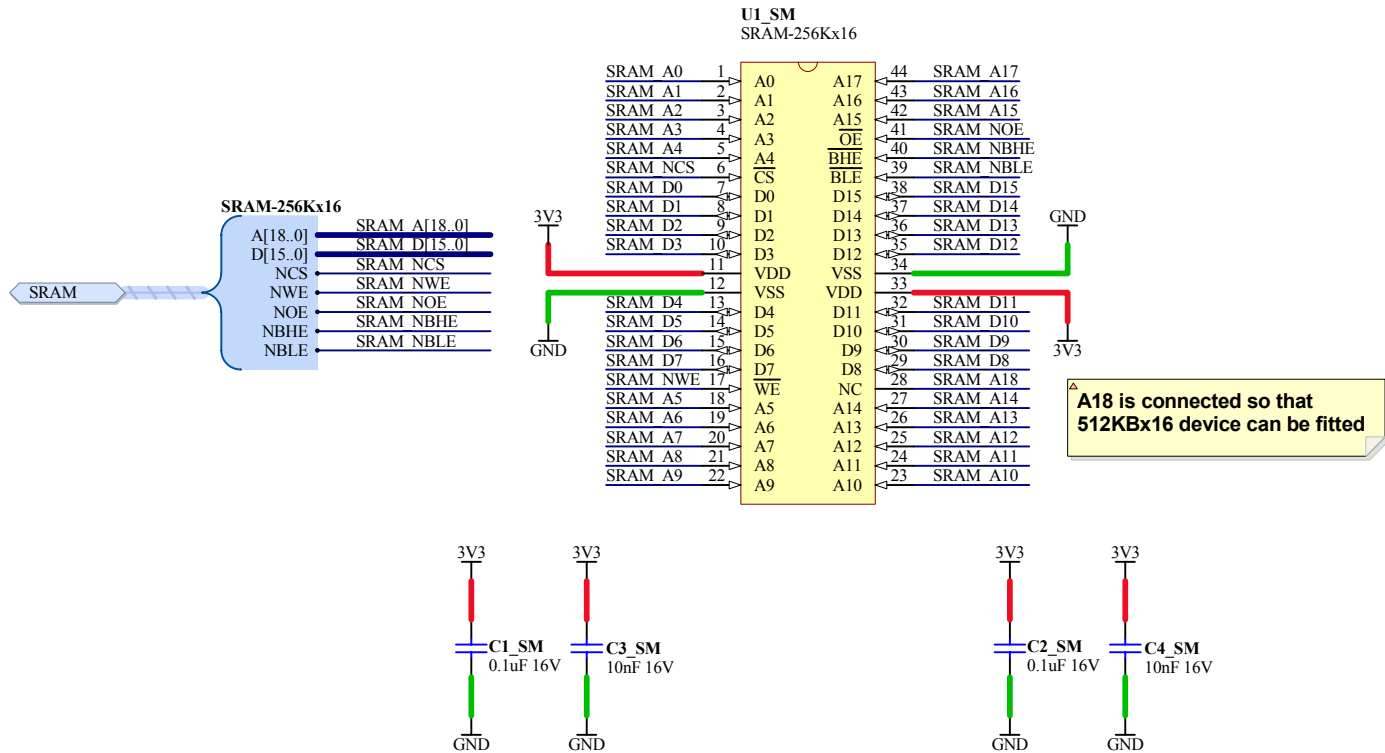
- all "power" resnets that terminate the FLASH-only signals (ie. RN1 and RN3).
- all "ground" resnets that terminate the FLASH-only signals (ie. RN2 and RN4).
- all "power" resnets that terminate the FLASH-SRAM-only signals (ie. RN5 and RN7).
- all "ground" resnets that terminate the FLASH-SRAM-only signals (ie. RN6 and RN8).
- all "power" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN9, RN11, RN13, RN15, RN17, RN19, RN21, RN23, RN25, RN27, RN29, RN31, RN33, RN35).
- all "ground" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN10, RN12, RN14, RN16, RN18, RN20, RN22, RN24, RN26, RN28, RN30, RN32, RN34, RN36).

To remove any confusion by the PCB assembler, the following devices have been deleted entirely from the design: RN1 to RN16, and RN17 to RN32.

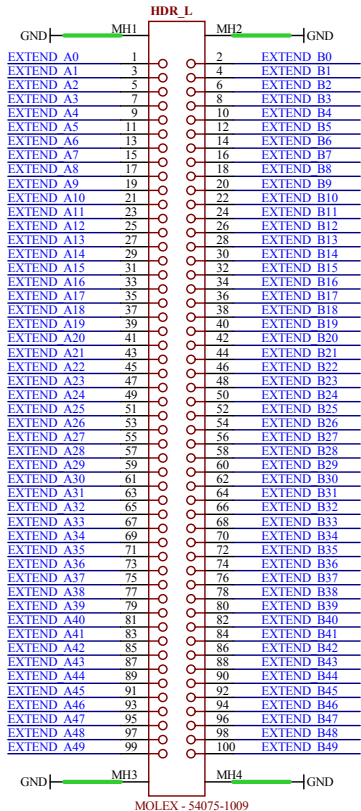
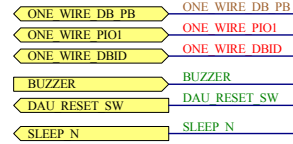
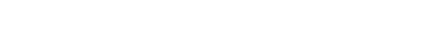
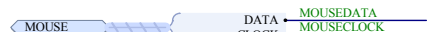
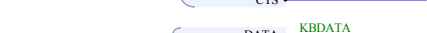
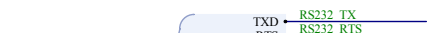
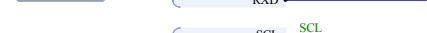
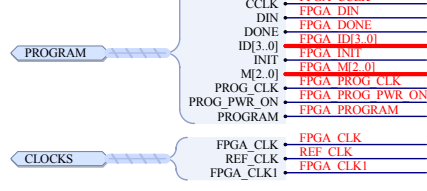
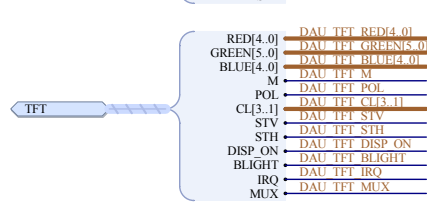
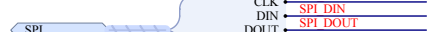
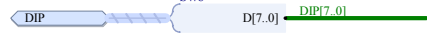
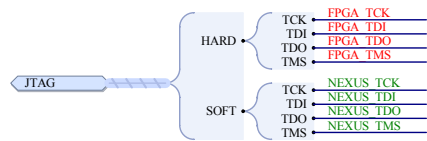
Note that high current (up to 1.25 Amps) is drawn from the 3V3 rail when all 19 pairs of resnets are loaded. The addition of up to 4.1 watts of heat was significantly warming the PCB.

Testing has confirmed that the loading of only 3 pairs of resnets (RN33/34, RN35/36 and RN37/38) provides good operation at speeds up to 96MHz. This consumes up to 0.20 amps, ie. up to 0.65 watts of heat.

The loading of the 3 pairs of resnets terminates only the output control signals from the FPGA to the SDRAM. The bidirectional data bus and address bus is not terminated. Signals that do not connect to the SDRAM (ie. signals to the slower flash and SRAM devices only) are also not terminated.



Sheet Title 256K x 16-Bit SRAM		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005			Revision:07
Date: 2/12/2008	Time: 1:17:15 PM			Sheet 18 of 21
File: SRAM 256Kx16 TSOP44.SchDoc				



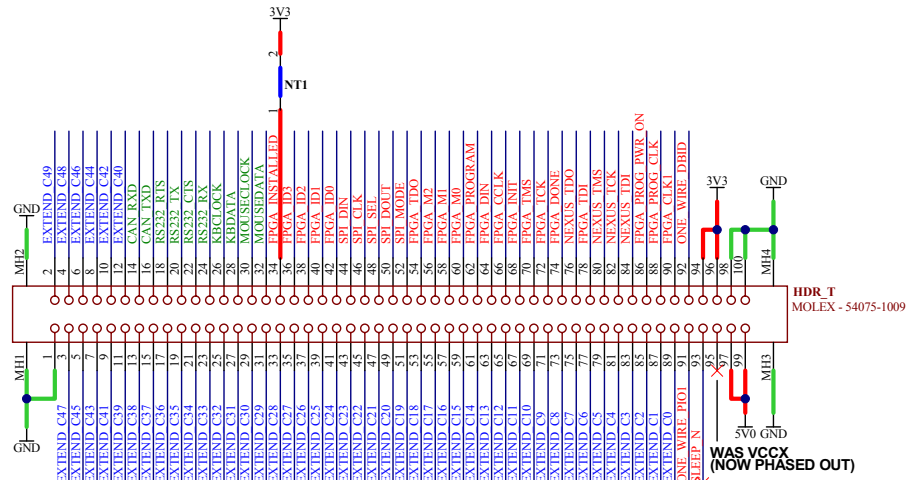
Red Connections are locked for NB1 compatibility. They are hardwired on the NB1 and therefore can NOT be changed.

Green connections are I/O pins connected to NB1 compatible PCB resources on the mother board. These can be changed.

Blue connections are connected to the New NB2 compatible resources on the motherboard. These can be changed.

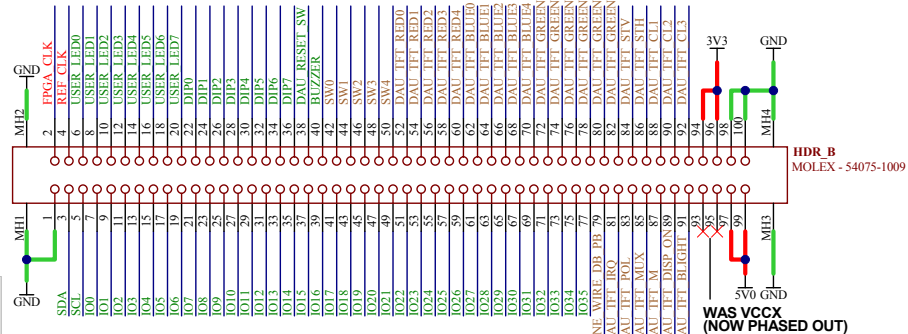
Note that the signal ONE_WIRE_DBID was previously called FPGA_CLK2.

This signal was included in NB1 design, but never used. Hence it has now been reallocated.



Note that the signal ONE_WIRE_DBID was previously called FPGA_CLK2.

This signal was included in NB1 design, but never used. Hence it has now been reallocated.



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U_MOUNTS
DB MOUNTS



PCB1
DB31 Blank PCB
Printed Circuit Board (Bare)

Sheet Title DB31 Hardware Kit			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB31 - Daughter Board Cyclone2				
Size: A4	Assy: D-820-0005	Revision:07		
Date: 2/12/2008	Time: 1:17:15 PM	Sheet 20 of 21		
File: DB31 Hardware Kit.SchDoc				

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B

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D

D

MH1
MOUNTING HOLE 3MM



MH2
MOUNTING HOLE 3MM



MH3
MOUNTING HOLE 3MM



Altium Logo Top1



Altium Logo Bot1



Sheet Title <i>Mounts, Logo & Label</i>		
Project Title <i>DB31 - Daughter Board Cyclone2</i>		
Size: A4	Assy: D-820-0005	Revision: 07
Date: 2/12/2008	Time: 1:17:15 PM	Sheet 21 of 21
File: DB_MOUNTS.SchDoc		

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Frenchs Forest
NSW 2086
Australia



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