

1

2

3

4

A

A

B

B

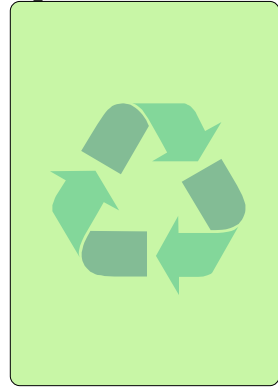
C

C

D

D

U_DB_Common
DB_Common



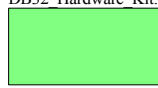
U_PSU
PSU.SCHDOC




U_Bypass_Board
DB_Bypass



U_DB32_Hardware_Kit
DB32_Hardware_Kit.SchDoc



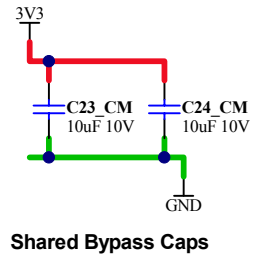
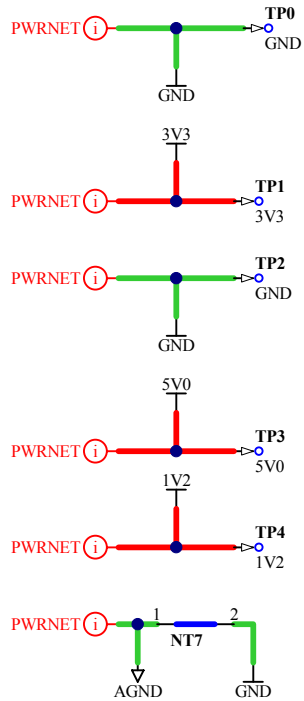
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Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006	Revision:08		
Date: 27/11/2008	Time: 2:12:55 PM	Sheet 1 of 21		
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1

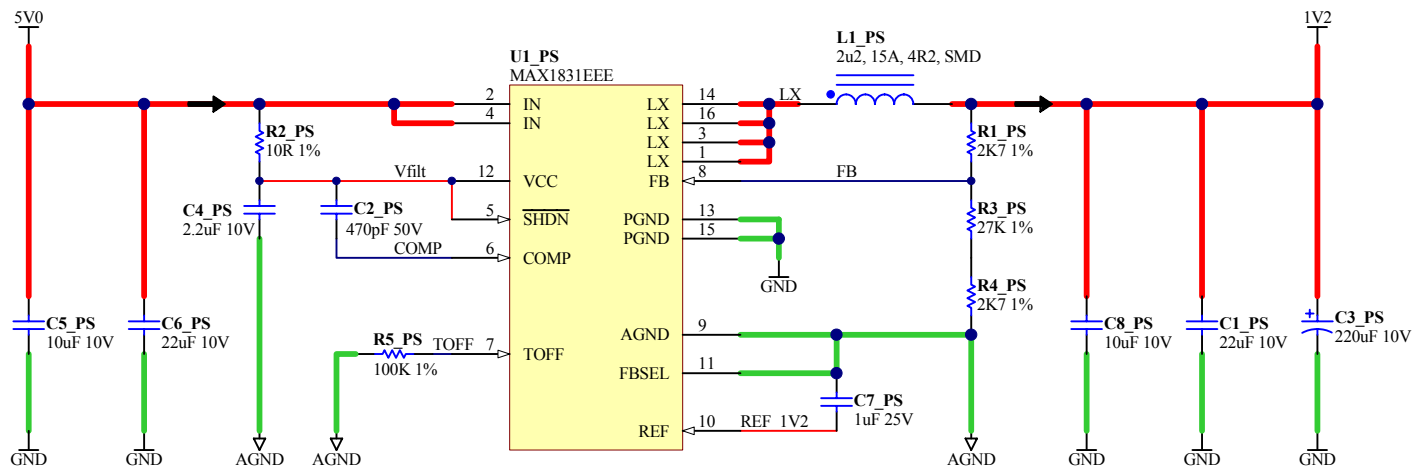
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3

4



Sheet Title Power Supply Top Level			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006	Revision:08		
Date: 27/11/2008	Time: 2:12:55 PM	Sheet 2 of 21		
File: PSU.SCHDOC				



Sheet Title **Power Supply MAX1831 (1V2)**

Project Title **DB32 - Daughter Board Lattice**

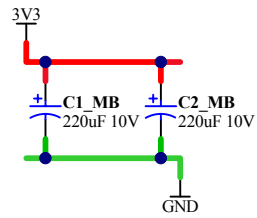
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Date: 27/11/2008 Time: 2:12:55 PM Sheet 3 of 21


File: PSU MAX1831 1V2 ALT.SchDoc

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Frenchs Forest
NSW 2086
Australia



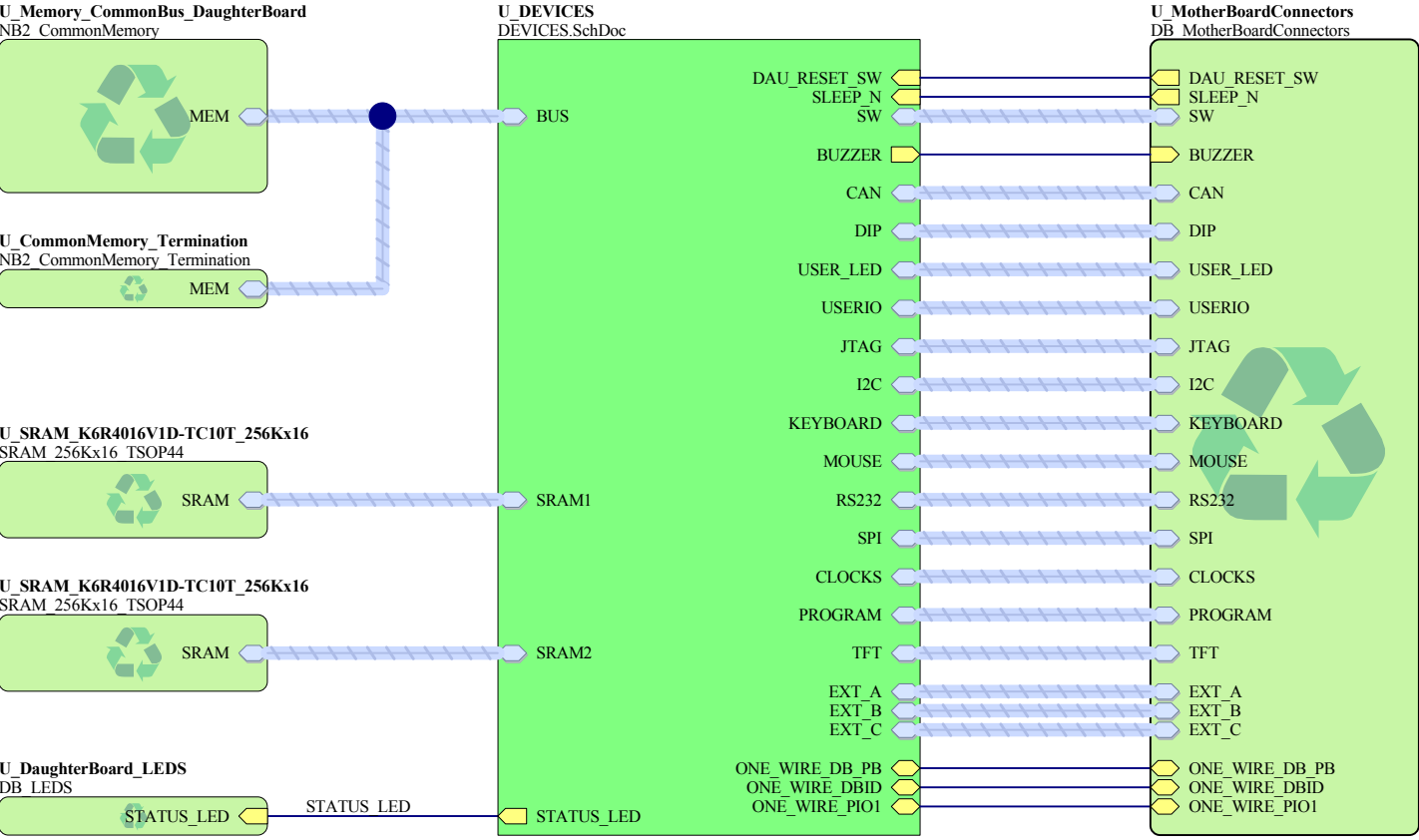


△ These decoupling capacitors are intended to assist the voltage rails on the PCB - where the decoupling capacitors for the FPGA are not close.

Sheet Title Board Bypass Capacitors			<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006	Revision:08		
Date: 27/11/2008	Time: 2:12:55 PM	Sheet 4 of 21		
File: DB Bypass.SchDoc				

**Top Level Schematic For Daughter Board Design
Both FPGA-Only and FPGA + MCU**

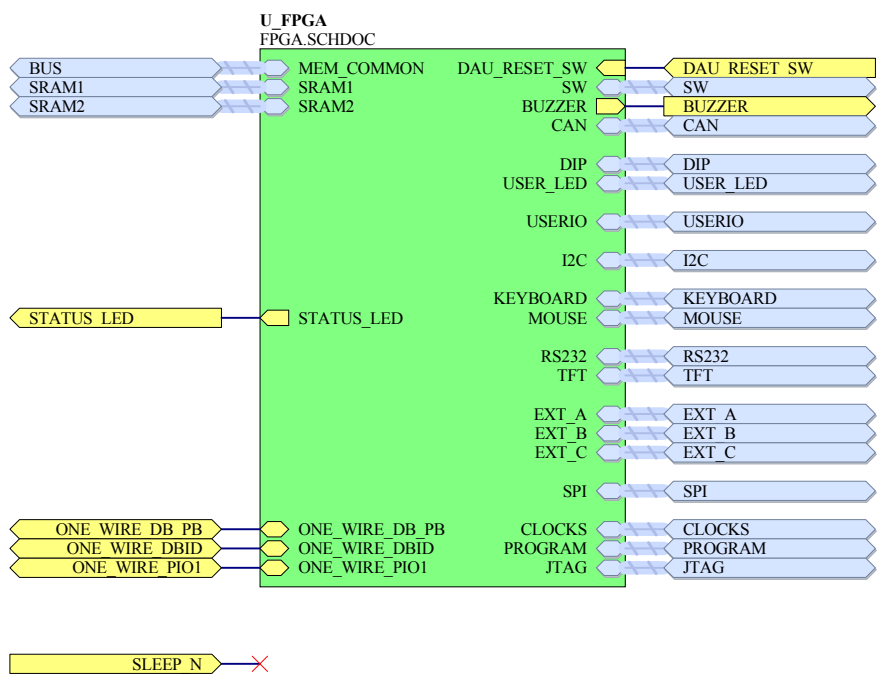
**This Device Sheet is the same for all designs.
It relies on being instantiated in a project that contains a device-specific sheet named DEVICES.SchDoc .**



Sheet Title Daughter Board Top Level		
Project Title DB32 - Daughter Board Lattice		
Size: A4	Assy: D-820-0006	Revision:08
Date: 27/11/2008	Time: 2:12:55 PM	Sheet 5 of 21
File: DB Common.SchDoc		

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Australia




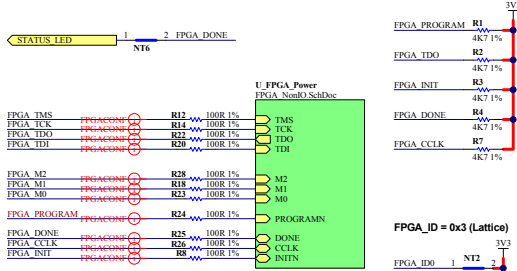


Device Specific Section of Daughter Board Design

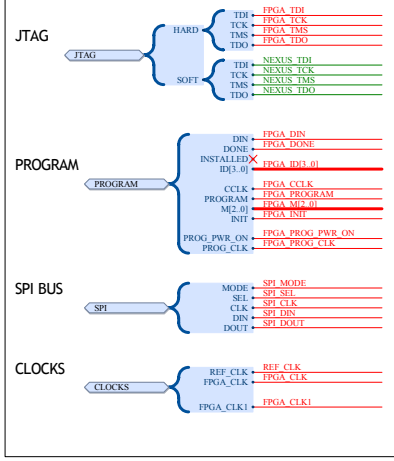
This schematic sheet (plus any child sheets) will contain the device specific parts of any daughter board designs.

This will include any FPGA or MCU devices as well as dedicated power supplies, connectors etc.

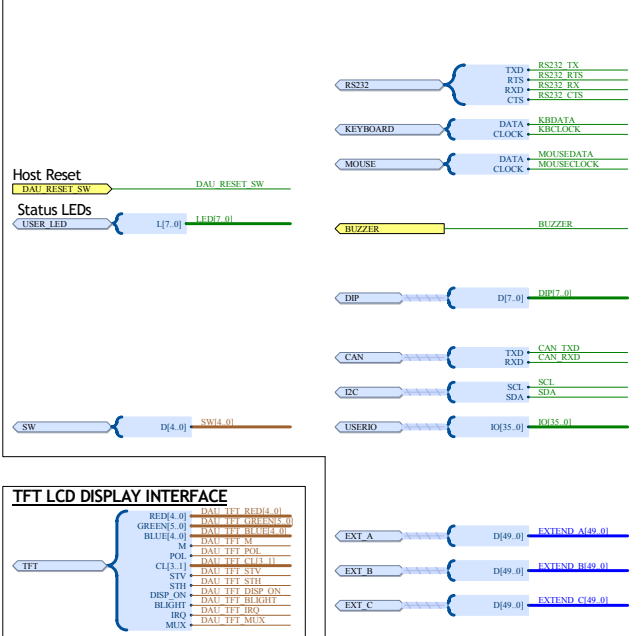
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Project Title DB32 - Daughter Board Lattice				
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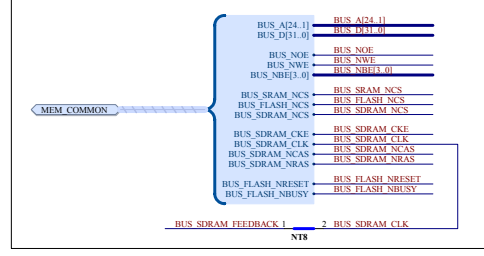
DAUGHTER BOARD I/O



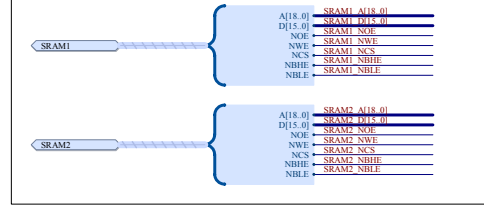
HOST PERIPHERALS



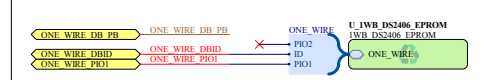
HOST MEMORY RESOURCES



DAUGHTER BOARD MEMORY RESOURCES

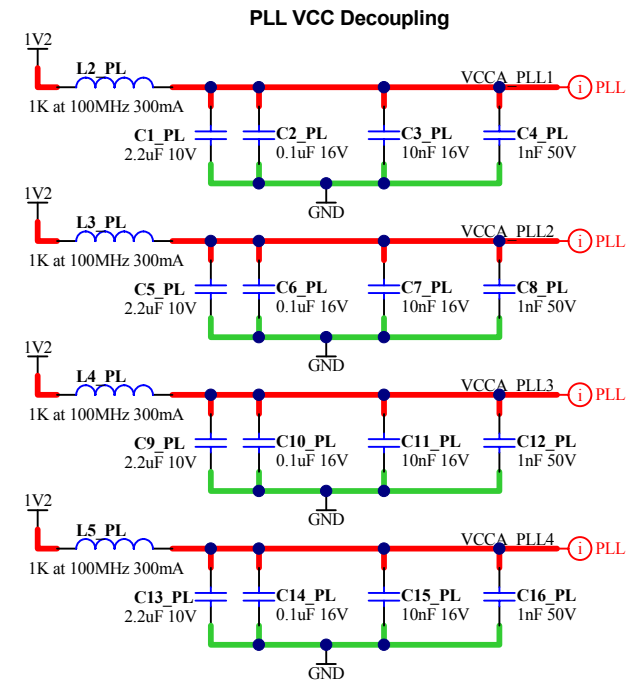
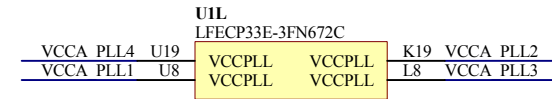
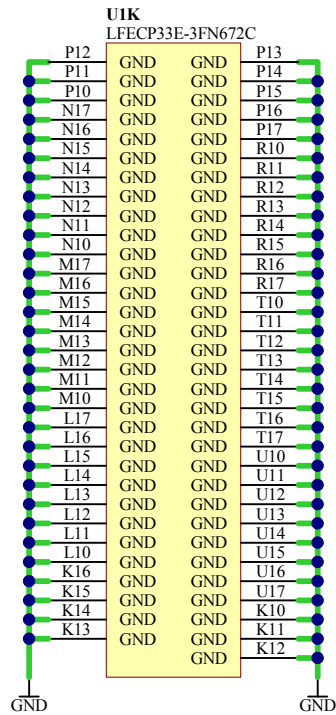
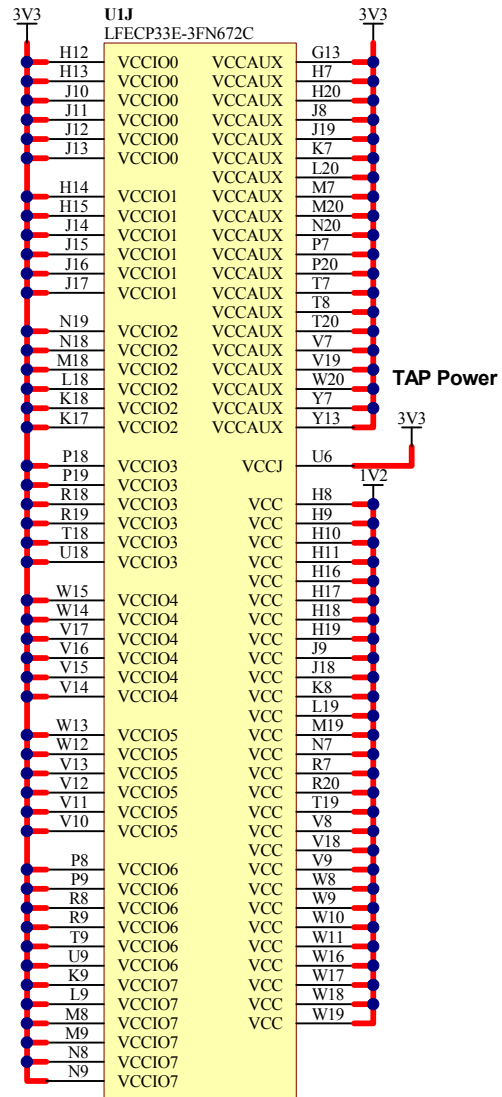
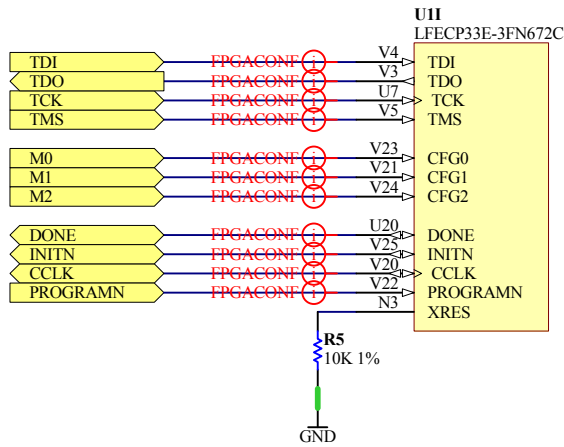


ONE-WIRE CONNECTIONS



NOTE: A = POSITIVE

U1A L1FCP33E-3FN672C	U1B L1FCP33E-3FN672C	U1C L1FCP33E-3FN672C	U1D L1FCP33E-3FN672C	U1E L1FCP33E-3FN672C	U1F L1FCP33E-3FN672C	U1G L1FCP33E-3FN672C	U1H L1FCP33E-3FN672C
BANK C P72A-16 P72B-17 P72C-18 P72D-19 P72E-20 P72F-21 P72G-22 P72H-23 P72I-24 P72J-25 P72K-26 P72L-27 P72M-28 P72N-29 P72O-30 P72P-31 P72Q-32 P72R-33 P72S-34 P72T-35 P72U-36 P72V-37 P72W-38 P72X-39 P72Y-40 P72Z-41 P73A-42 P73B-43 P73C-44 P73D-45 P73E-46 P73F-47 P73G-48 P73H-49 P73I-50 P73J-51 P73K-52 P73L-53 P73M-54 P73N-55 P73O-56 P73P-57 P73Q-58 P73R-59 P73S-60 P73T-61 P73U-62 P73V-63 P73W-64 P73X-65 P73Y-66 P73Z-67 P74A-68 P74B-69 P74C-70 P74D-71 P74E-72 P74F-73 P74G-74 P74H-75 P74I-76 P74J-77 P74K-78 P74L-79 P74M-80 P74N-81 P74O-82 P74P-83 P74Q-84 P74R-85 P74S-86 P74T-87 P74U-88 P74V-89 P74W-90 P74X-91 P74Y-92 P74Z-93 P75A-94 P75B-95 P75C-96 P75D-97 P75E-98 P75F-99 P75G-100 P75H-101 P75I-102 P75J-103 P75K-104 P75L-105 P75M-106 P75N-107 P75O-108 P75P-109 P75Q-110 P75R-111 P75S-112 P75T-113 P75U-114 P75V-115 P75W-116 P75X-117 P75Y-118 P75Z-119 P76A-120 P76B-121 P76C-122 P76D-123 P76E-124 P76F-125 P76G-126 P76H-127 P76I-128 P76J-129 P76K-130 P76L-131 P76M-132 P76N-133 P76O-134 P76P-135 P76Q-136 P76R-137 P76S-138 P76T-139 P76U-140 P76V-141 P76W-142 P76X-143 P76Y-144 P76Z-145 P77A-146 P77B-147 P77C-148 P77D-149 P77E-150 P77F-151 P77G-152 P77H-153 P77I-154 P77J-155 P77K-156 P77L-157 P77M-158 P77N-159 P77O-160 P77P-161 P77Q-162 P77R-163 P77S-164 P77T-165 P77U-166 P77V-167 P77W-168 P77X-169 P77Y-170 P77Z-171 P78A-172 P78B-173 P78C-174 P78D-175 P78E-176 P78F-177 P78G-178 P78H-179 P78I-180 P78J-181 P78K-182 P78L-183 P78M-184 P78N-185 P78O-186 P78P-187 P78Q-188 P78R-189 P78S-190 P78T-191 P78U-192 P78V-193 P78W-194 P78X-195 P78Y-196 P78Z-197 P79A-198 P79B-199 P79C-200 P79D-201 P79E-202 P79F-203 P79G-204 P79H-205 P79I-206 P79J-207 P79K-208 P79L-209 P79M-210 P79N-211 P79O-212 P79P-213 P79Q-214 P79R-215 P79S-216 P79T-217 P79U-218 P79V-219 P79W-220 P79X-221 P79Y-222 P79Z-223 P80A-224 P80B-225 P80C-226 P80D-227 P80E-228 P80F-229 P80G-230 P80H-231 P80I-232 P80J-233 P80K-234 P80L-235 P80M-236 P80N-237 P80O-238 P80P-239 P80Q-240 P80R-241 P80S-242 P80T-243 P80U-244 P80V-245 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P113E-1086 P113F-1087 P113G-1088 P113H-1089 P113I-1090 P113J-1091 P113K-1092 P113L-1093 P113M-1094 P113N-1095 P113O-1096 P113P-1097 P113Q-1098 P113R-1099 P113S-1100 P113T-1101 P113U-1102							



Sheet Title **FPGA Power and Programming**

Project Title **DB32 - Daughter Board Lattice**

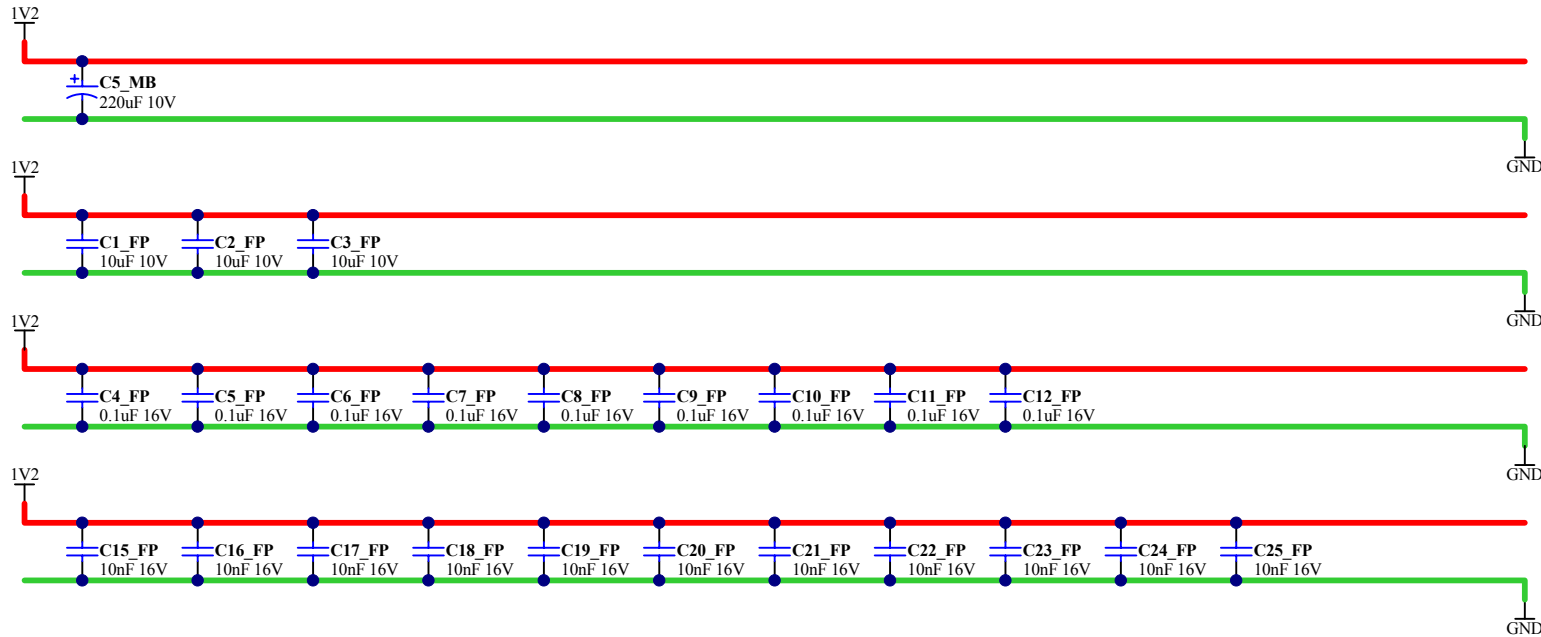
Size: A4 Assy: D-820-0006 Revision: 08


Date: 27/11/2008 Time: 2:12:56 PM Sheet 8 of 21

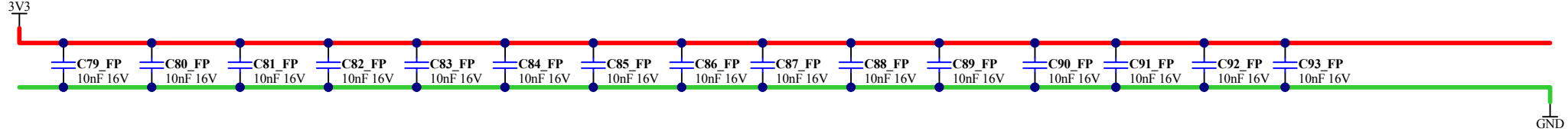
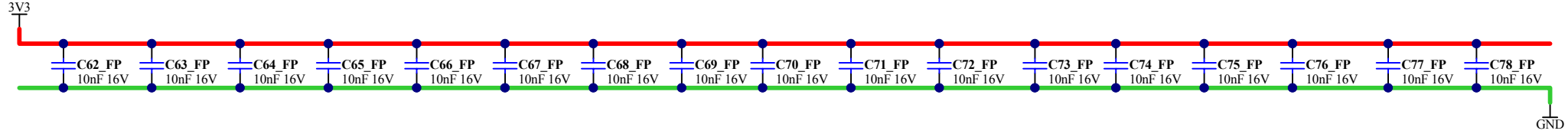
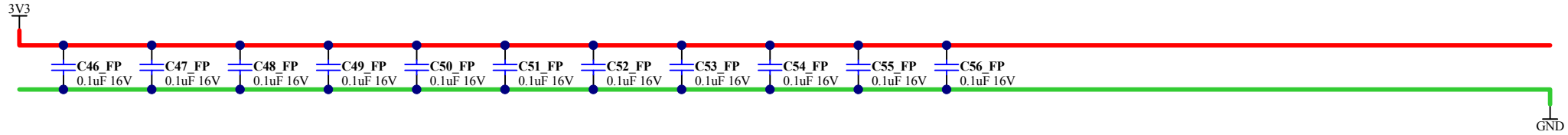
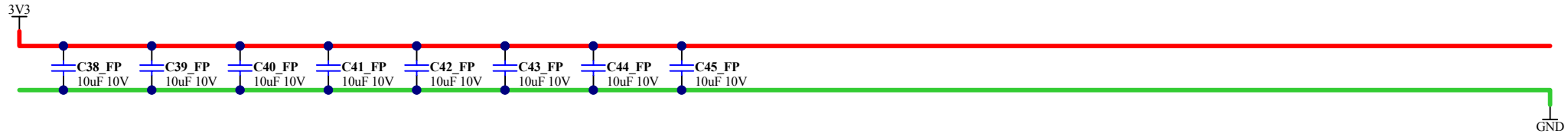
File: FPGA_NonIO.SchDoc


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NSW 2086
Australia

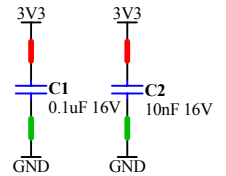
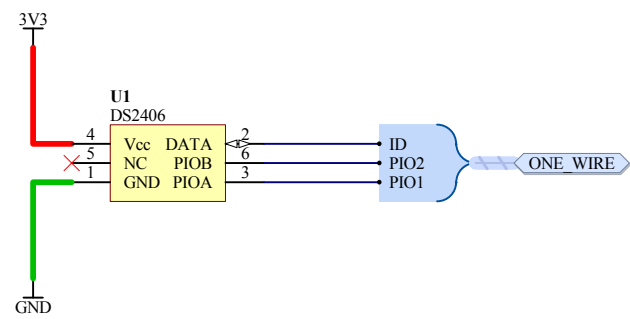





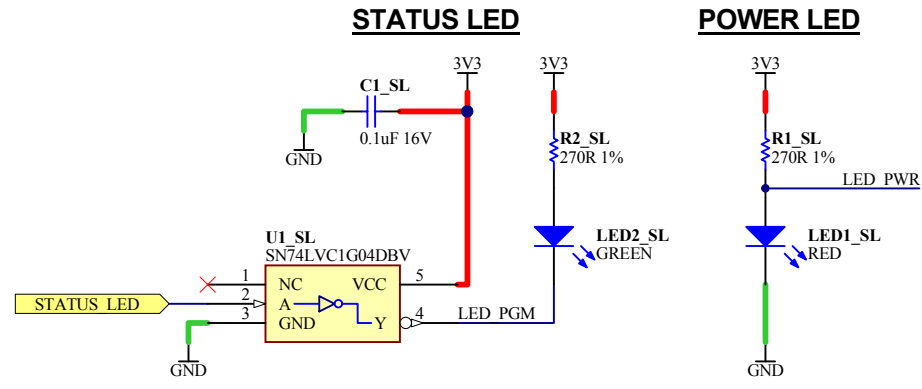
Sheet Title FPGA Bypass Capacitors for 1V2		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006			Revision:08
Date: 27/11/2008	Time: 2:12:56 PM			Sheet 9 of 21
File: Bypass FPGA 1V2.SCHDOC				




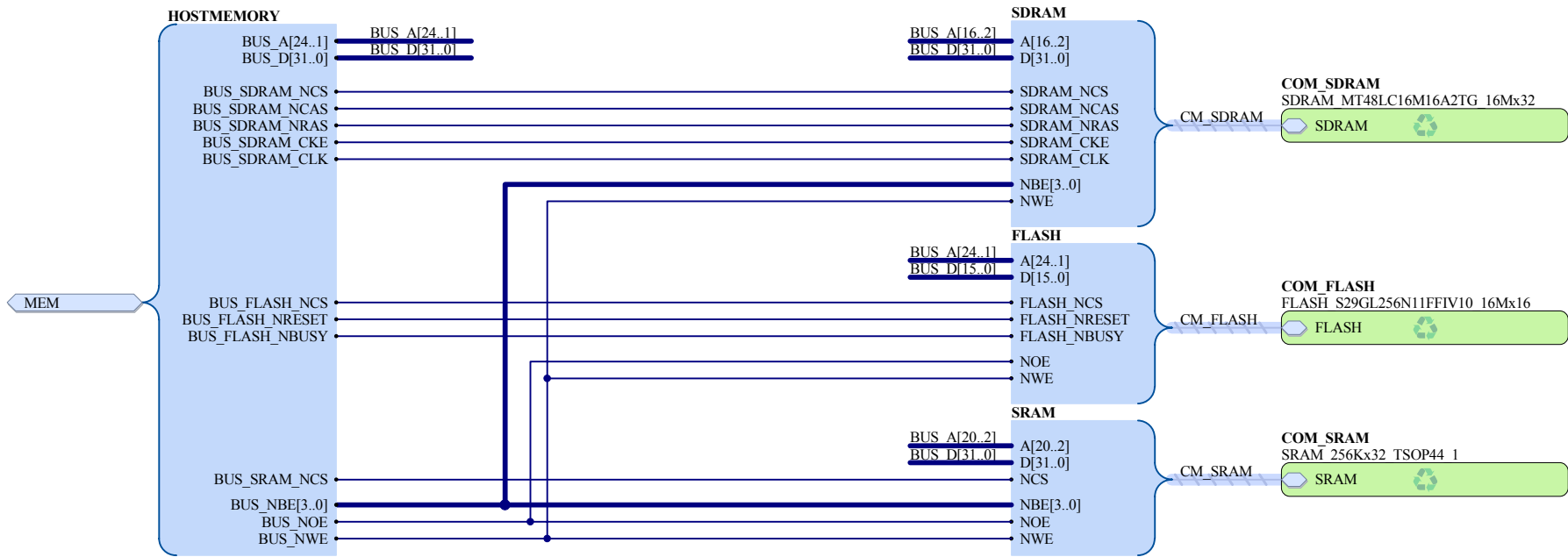
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Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006			Revision:08
Date: 27/11/2008	Time: 2:12:56 PM			Sheet 10 of 21
File: Bypass FPGA 3V3.SchDoc				




Sheet Title <i>1-Wire Bus ID</i>			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title <i>DB32 - Daughter Board Lattice</i>				
Size: A4	Assy: D-820-0006	Revision:08		
Date: 27/11/2008	Time: 2:12:56 PM	Sheet 11 of 21		
File: 1WB_DS2406_EPROM.SchDoc				



Sheet Title Daughter Board LEDs		<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006			Revision:08
Date: 27/11/2008	Time: 2:12:56 PM			Sheet 12 of 21
File: DB_LEDS.SchDoc				



Common-Bus Memory Block
256K x 32-bit SRAM (1 MByte)
16M x 32-Bit SDRAM (64 MByte)
16M x 16-Bit Flash (32 MByte)

Sheet Title Common-Bus Memory Block			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006	Revision: 08		
Date: 27/11/2008	Time: 2:12:56 PM	Sheet 13 of 21		
File: NB2_CommonMemory.SchDoc				

1

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A

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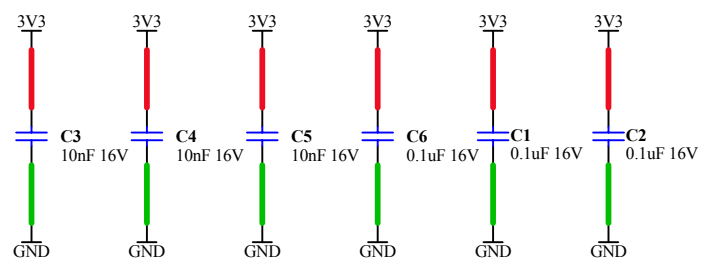
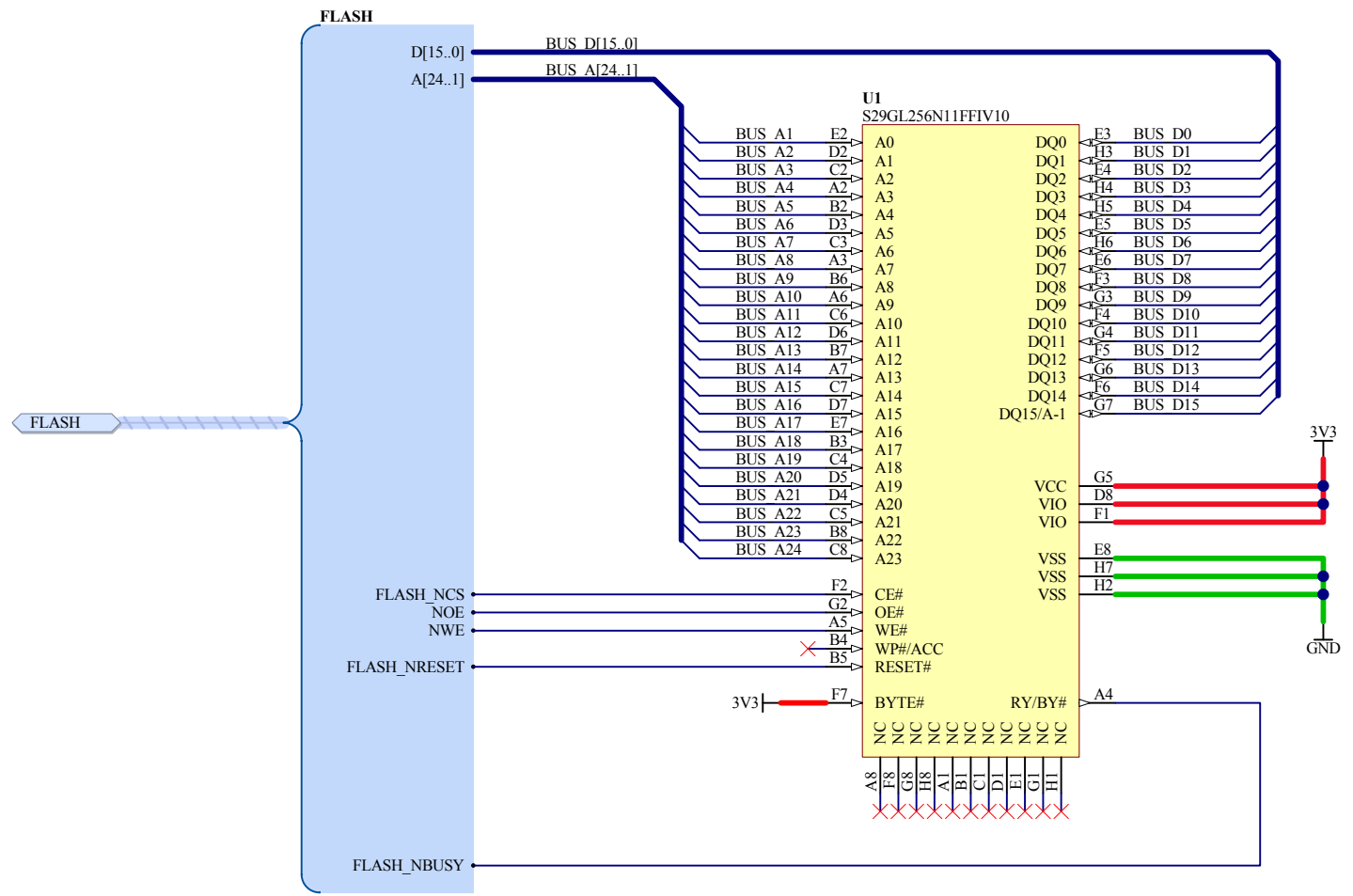
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1

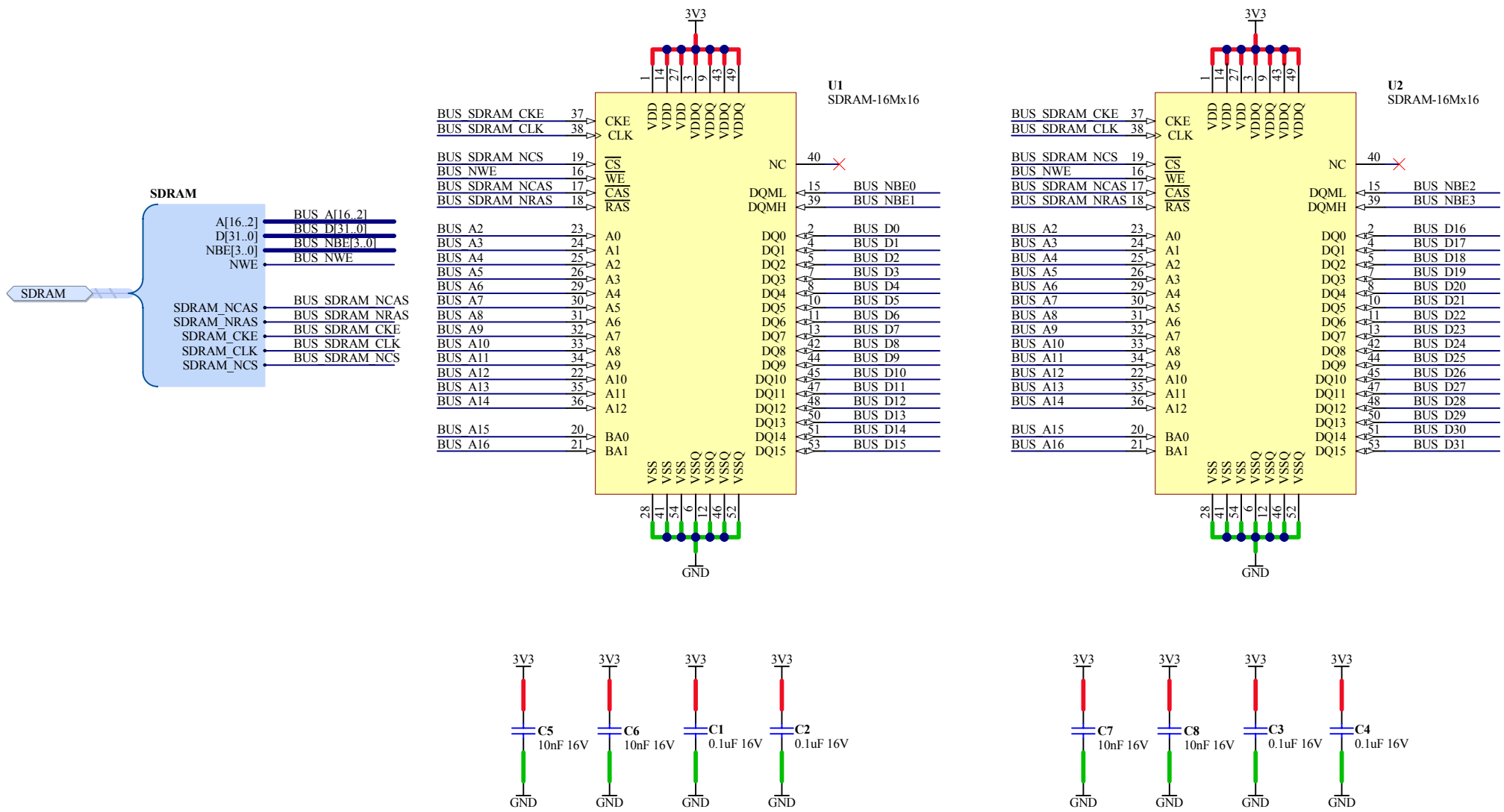
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3

4

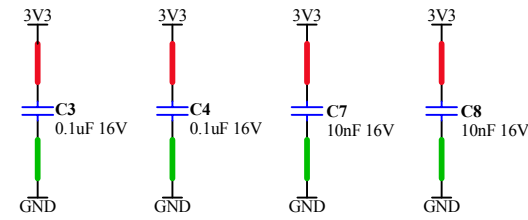
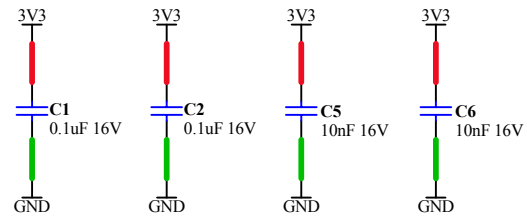
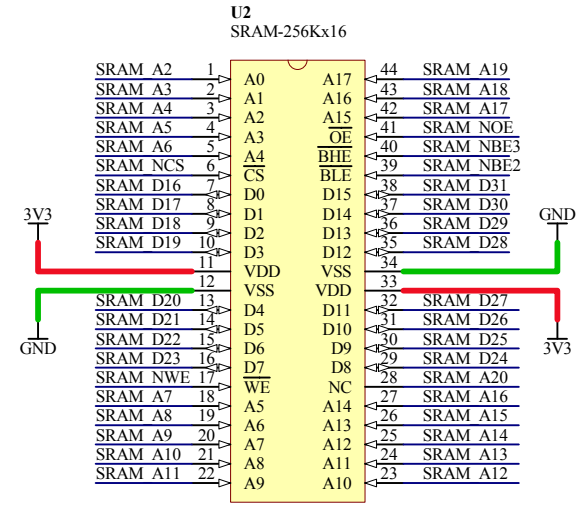
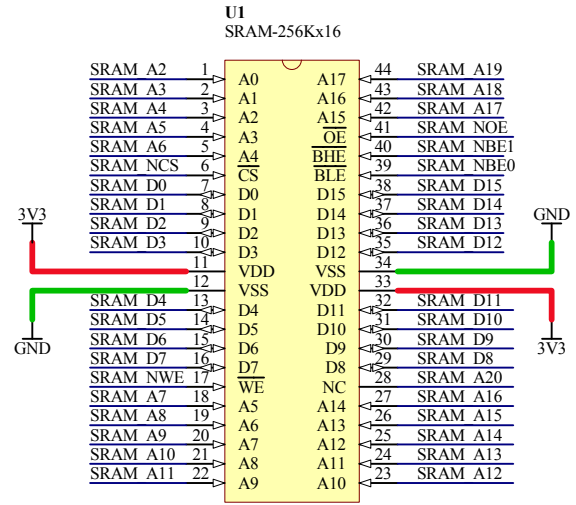
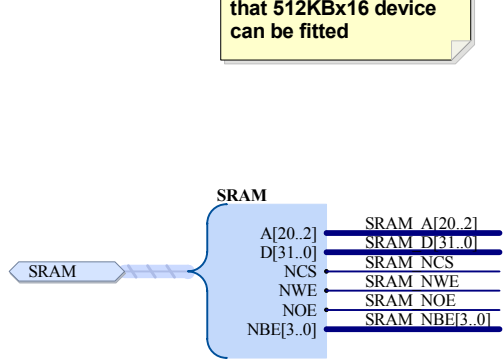


Sheet Title 16M x 16 Flash Memory (BGA)			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006	Revision: 08		
Date: 27/11/2008	Time: 2:12:56 PM	Sheet 14 of 21		
File: FLASH_S29GL256N11FFIV10_16Mx16.SchDoc				

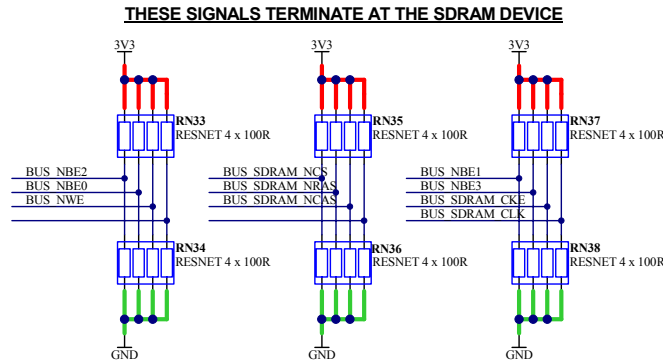
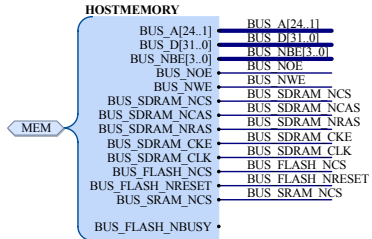


Sheet Title 16M x 32 SDRAM TSOP54 x 2			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006	Revision: 08		
Date: 27/11/2008	Time: 2:12:56 PM	Sheet 15 of 21		
File: SDRAM_MT48LC16M16A2TG_16Mx32.SchDoc				

A18 is connected so that 512KBx16 device can be fitted



Sheet Title 256K x 32 SRAM - TSOP44 x 2		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice			
Size: A4	Assy: D-820-0006	Revision: 08	
Date: 27/11/2008	Time: 2:12:56 PM	Sheet 16 of 21	
File: SRAM 256Kx32 TSOP44 1.SchDoc			



All devices using controlled impedance outputs from the source (ie. FPGA) should use 50 ohm (2 parallel 100 ohm resistors) termination.

The Flash should be located closest to the source (FPGA).

The SRAM should be located next furthest from the source (FPGA).

The SDRAM should be located next furthest from the source (FPGA).

Terminations are to be located at the furthest distance from the source (FPGA).

Note that pins 5,6,7 and 8 of the following resnet "groups" are pin-swappable within that "group":

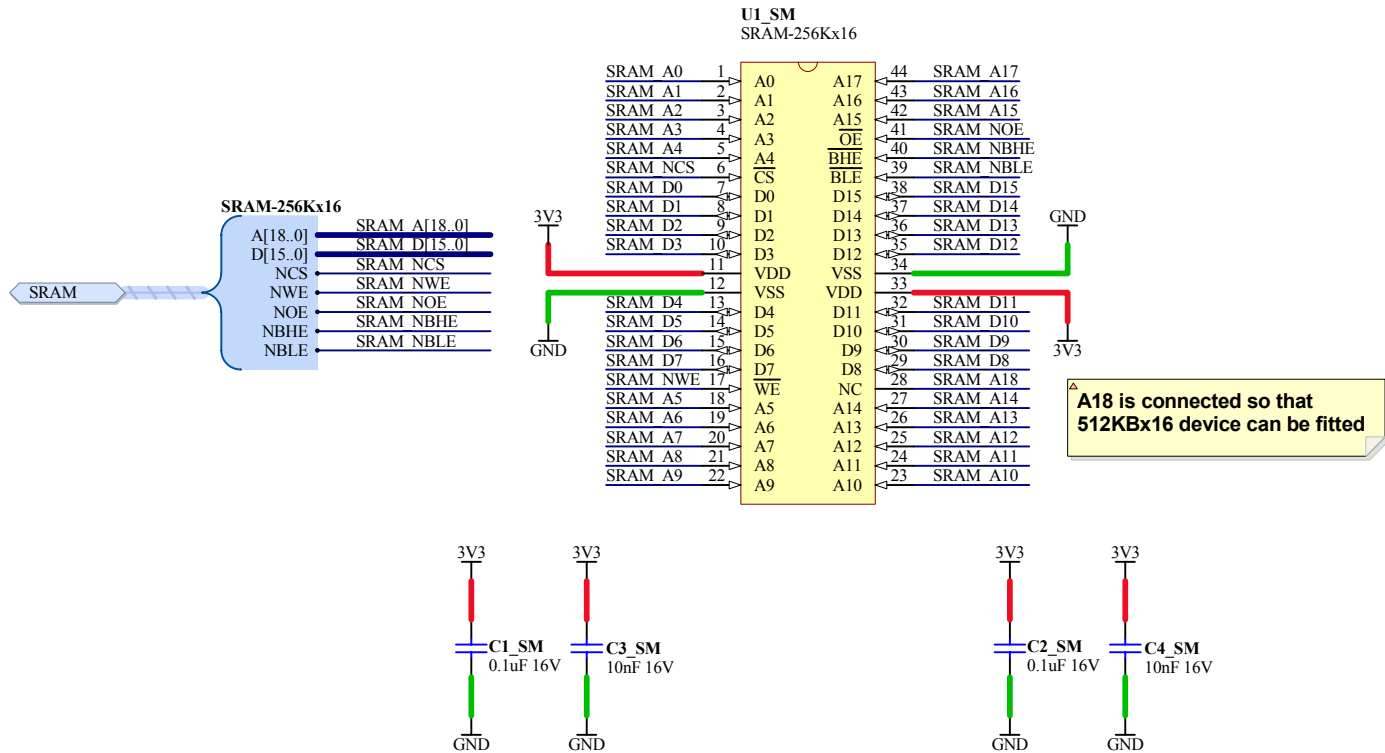
- all "power" resnets that terminate the FLASH-only signals (ie. RN1 and RN3).
- all "ground" resnets that terminate the FLASH-only signals (ie. RN2 and RN4).
- all "power" resnets that terminate the FLASH-SRAM-only signals (ie. RN5 and RN7).
- all "ground" resnets that terminate the FLASH-SRAM-only signals (ie. RN6 and RN8).
- all "power" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN9, RN11, RN13, RN15, RN17, RN19, RN21, RN23, RN25, RN27, RN29, RN31, RN33, RN35).
- all "ground" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN10, RN12, RN14, RN16, RN18, RN20, RN22, RN24, RN26, RN28, RN30, RN32, RN34, RN36).

To remove any confusion by the PCB assembler, the following devices have been deleted entirely from the design: RN1 to RN16, and RN17 to RN32.

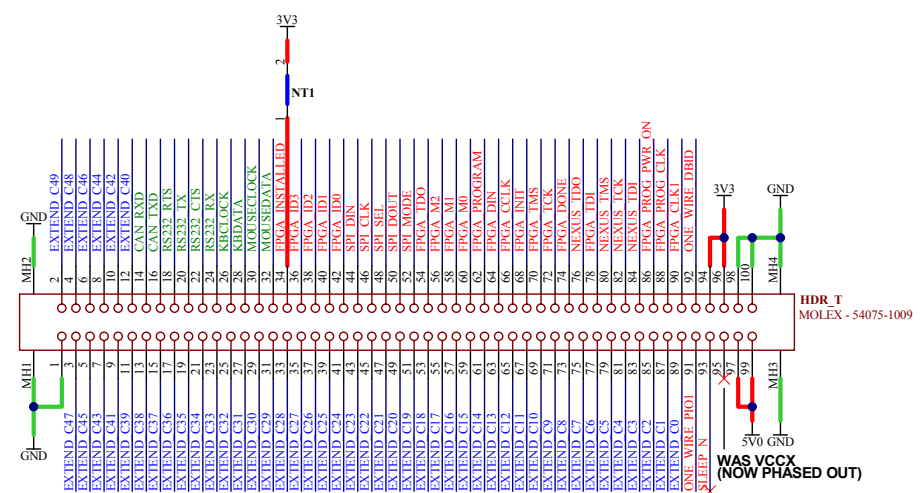
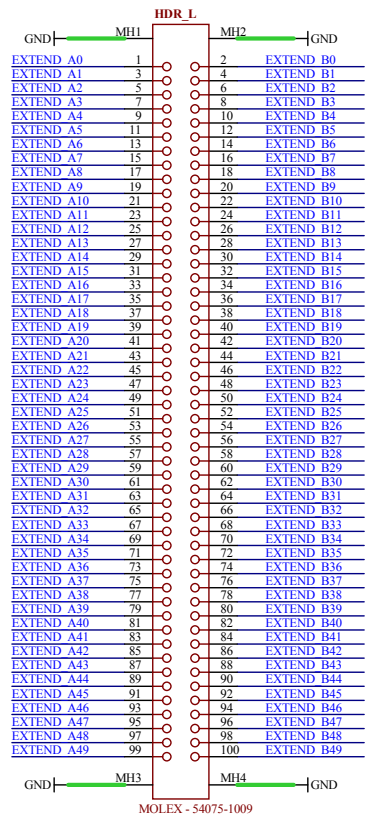
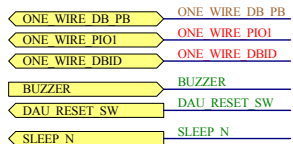
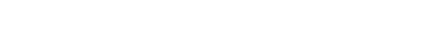
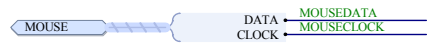
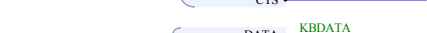
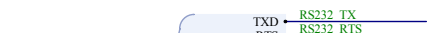
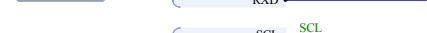
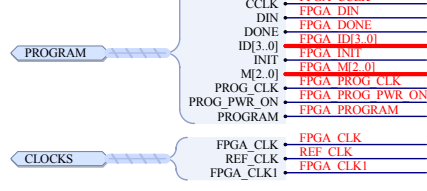
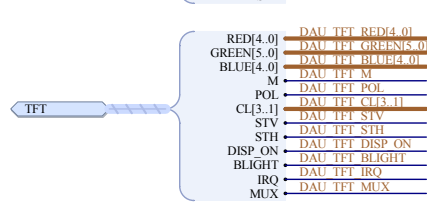
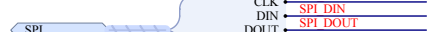
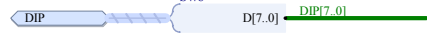
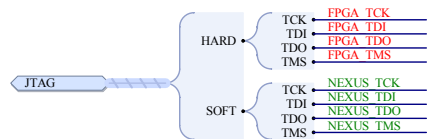
Note that high current (up to 1.25 Amps) is drawn from the 3V3 rail when all 19 pairs of resnets are loaded. The addition of up to 4.1 watts of heat was significantly warming the PCB.

Testing has confirmed that the loading of only 3 pairs of resnets (RN33/34, RN35/36 and RN37/38) provides good operation at speeds up to 96MHz. This consumes up to 0.20 amps, ie. up to 0.65 watts of heat.

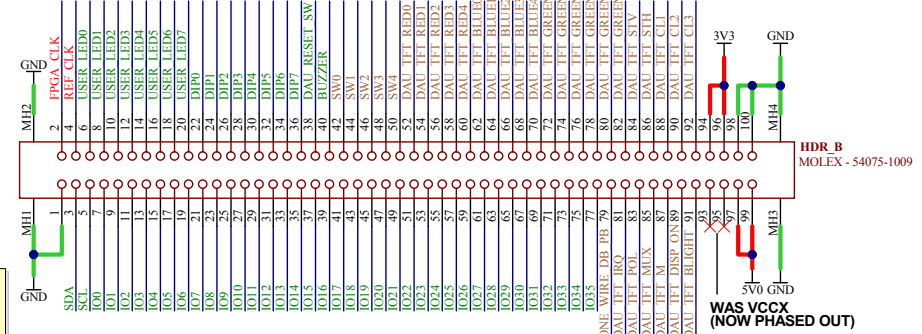
The loading of the 3 pairs of resnets terminates only the output control signals from the FPGA to the SDRAM. The bidirectional data bus and address bus is not terminated. Signals that do not connect to the SDRAM (ie. signals to the slower flash and SRAM devices only) are also not terminated.



Sheet Title 256K x 16-Bit SRAM		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice			
Size: A4	Assy: D-820-0006	Revision:08	
Date: 27/11/2008	Time: 2:12:56 PM	Sheet 18 of 21	
File: SRAM 256Kx16 TSOP44.SchDoc			



Note that the signal ONE_WIRE_DBID was previously called FPGA_CLK2. This signal was included in NB1 design, but never used. Hence it has now been reallocated.



Red Connections are locked for NB1 compatibility. They are hardwired on the NB1 and therefore can NOT be changed.

Green connections are I/O pins connected to NB1 compatible PCB resources on the mother board. These can be changed.

Blue connections are connected to the New NB2 compatible resources on the mother board. These can be changed.

1

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4

A

A

B

B

C

C


D

D

U_MOUNTS
DB MOUNTS



PCB1
DB32 Blank PCB
Printed Circuit Board (Bare)

Sheet Title DB32 Hardware Kit			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB32 - Daughter Board Lattice				
Size: A4	Assy: D-820-0006	Revision:08		
Date: 27/11/2008	Time: 2:12:56 PM	Sheet 20 of 21		
File: DB32 Hardware Kit.SchDoc				

1

2

3

4

1

2

3

4

A

A

B

B

C

C

D

D

MH1
MOUNTING HOLE 3MM



MH2
MOUNTING HOLE 3MM



MH3
MOUNTING HOLE 3MM



Altium Logo Top1



Altium Logo Bot1

Sheet Title ***Mounts, Logo & Label***

Project Title ***DB32 - Daughter Board Lattice***

Size: **A4** Assy: **D-820-0006** Revision: **08**

Date: **27/11/2008** Time: **2:12:56 PM** Sheet **21** of **21**

File: **DB_MOUNTS.SchDoc**

Altium Limited
*L3, 12A Rodborough Road
Frenchs Forest
NSW 2086
Australia*



1

2

3

4