

1

2

3

4

A

A

B

B

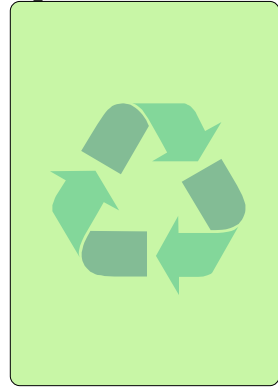
C

C

D

D

U_DB_Common
DB_Common



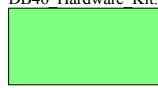
U_PSU
PSU.SCHDOC




U_Bypass_Board
DB_Bypass



U_DB46_Hardware_Kit
DB46_Hardware_Kit.SchDoc



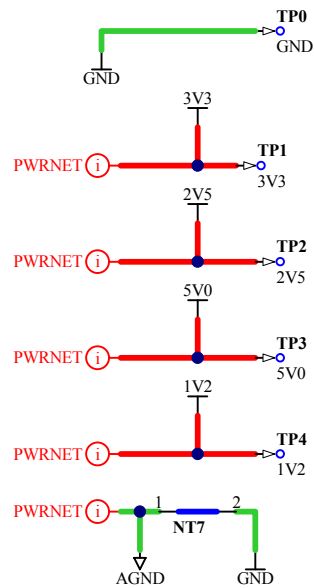
Sheet Title DB46 Top Level			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision:02		
Date: 27/11/2008	Time: 4:51:03 PM	Sheet 1 of 23		
File: DB46_Top.SchDoc				

1

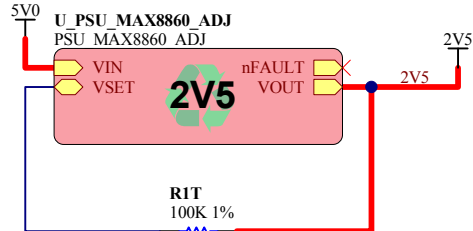
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3

4

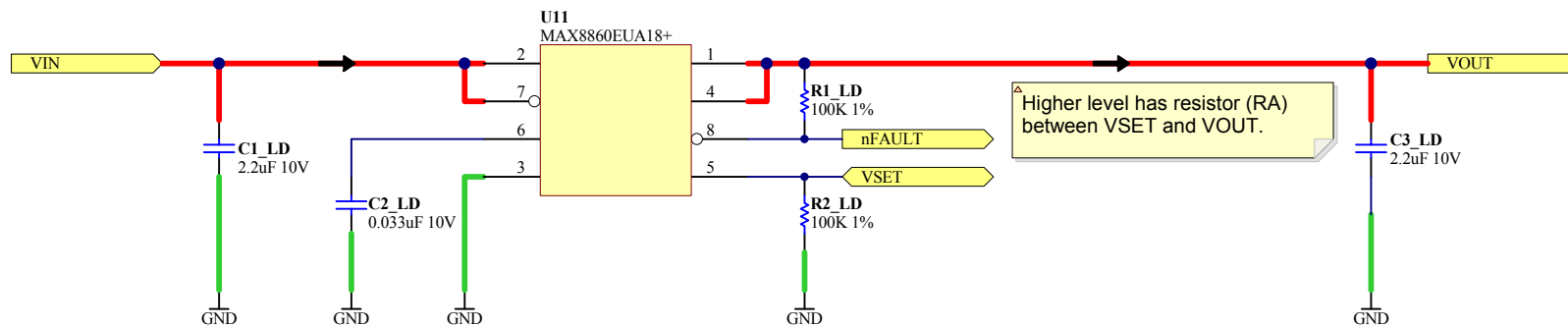


U_PSU_MAX1831_1V2_ALT
PSU MAX1831 1V2 ALT



^a Analog power for the FPGA VCCAUX is set to a nominal 2.5V by the 100K feedback resistor.

Sheet Title Power Supply Top Level			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision:02		
Date: 27/11/2008	Time: 4:51:03 PM	Sheet 2 of 23		
File: PSU.SCHDOC				



Higher level has resistor (RA) between VSET and VOUT.

The voltage provided by the MAX8860 linear regulator is determined by the addition of a resistor between VOUT and VSET.

This additional resistor (RA) is located on the higher-level schematic.

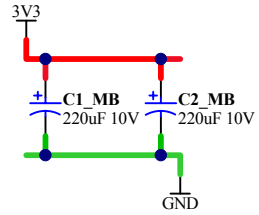
The voltage produced by the MAX8860 is calculated as follows:
 $VOUT = 1.25 * (1 + RA / 100k)$

If RA = 20k, $VOUT = 1.25 * (1 + 20k/100k) = 1.50$ Volts
 If RA = 100k, $VOUT = 1.25 * (1 + 100k/100k) = 2.50$ Volts
 If RA = 164k, $VOUT = 1.25 * (1 + 164k/100k) = 3.30$ Volts


Note that if VSET is grounded (on the higher-level schematic), VOUT=1.8 Volts

Note also that VIN must be a minimum of 0.18 Volts above VOUT.

Sheet Title Power Supply MAX8860 (2V5)		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35			
Size: A4	Assy: D-820-0031	Revision:02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 4 of 23	
File: PSU_MAX8860_ADJ.SchDoc			

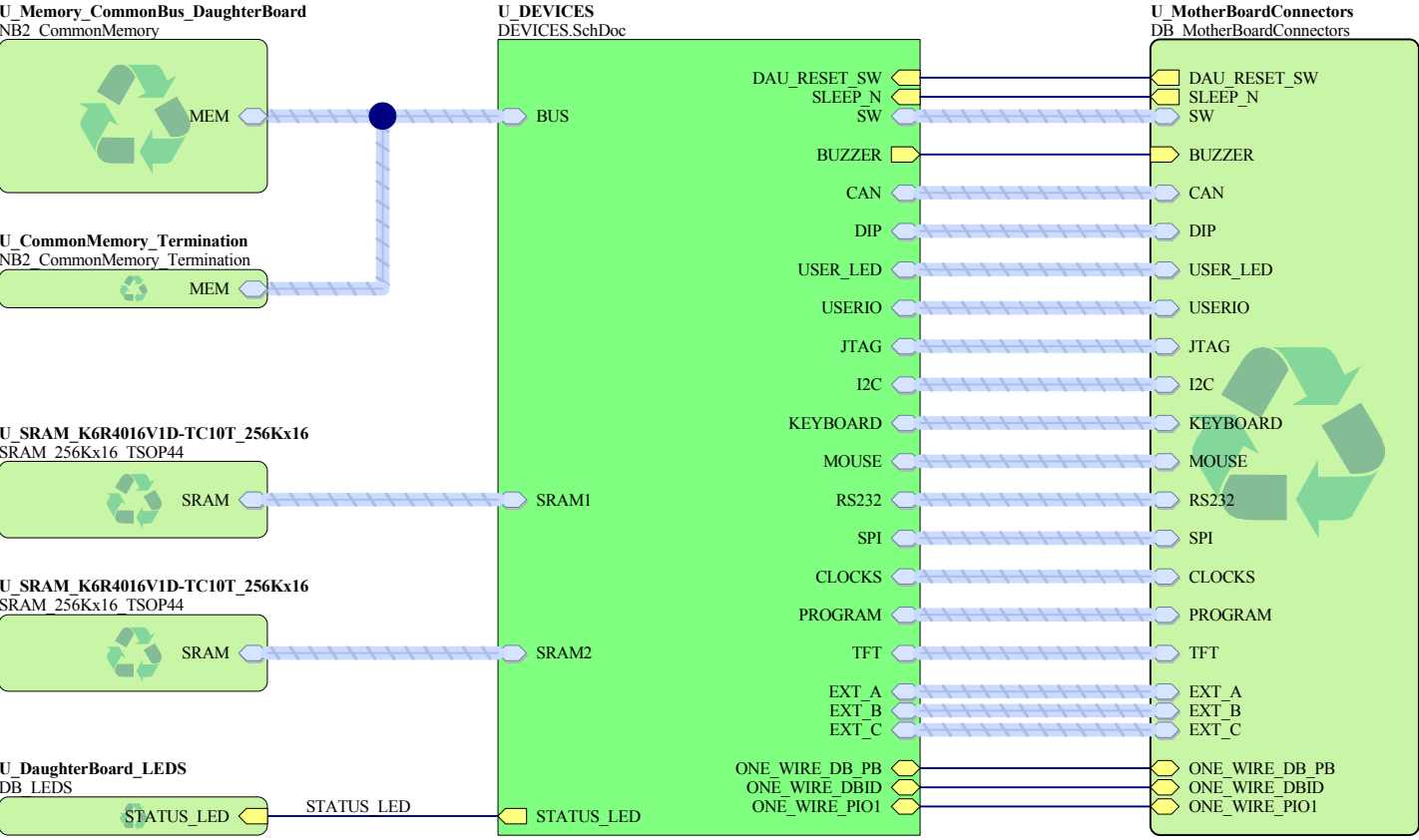


△ These decoupling capacitors are intended to assist the voltage rails on the PCB - where the decoupling capacitors for the FPGA are not close.

Sheet Title Board Bypass Capacitors			<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision:02		
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 5 of 23		
File: DB Bypass.SchDoc				

**Top Level Schematic For Daughter Board Design
Both FPGA-Only and FPGA + MCU**

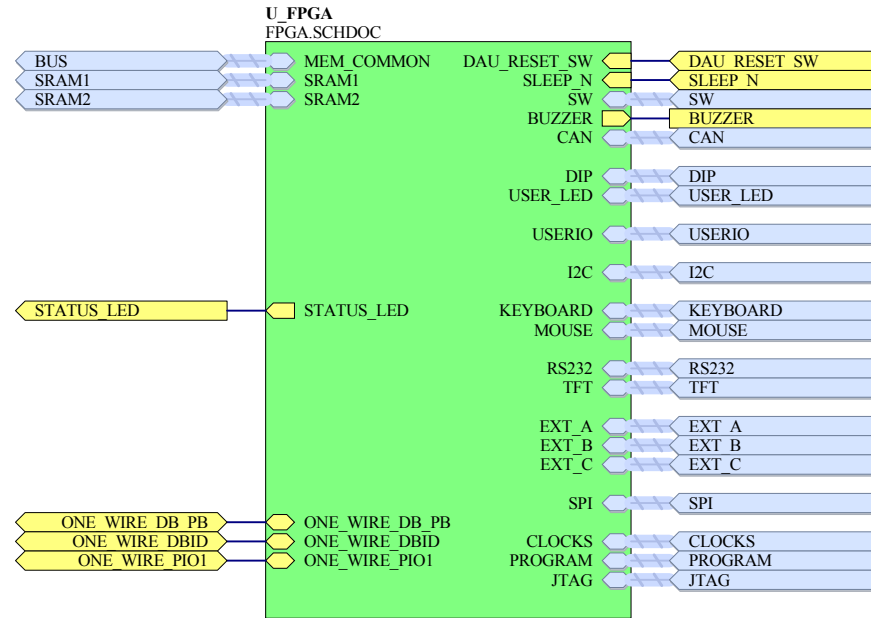
**This Device Sheet is the same for all designs.
It relies on being instantiated in a project that contains a device-specific sheet named DEVICES.SchDoc .**



Sheet Title Daughter Board Top Level		
Project Title DB46 - Virtex4 SX35		
Size: A4	Assy: D-820-0031	Revision:02
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 6 of 23
File: DB Common.SchDoc		

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NSW 2086
Australia





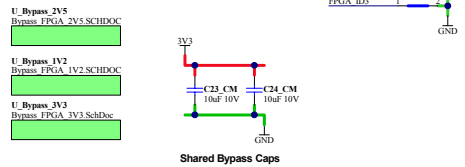
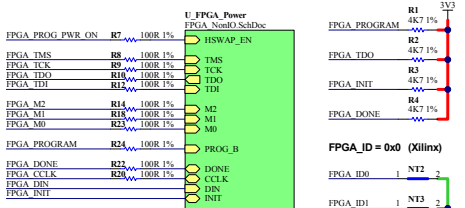
Device Specific Section of Daughter Board Design

This schematic sheet (plus any child sheets) will contain the device specific parts of any daughter board designs.

This will include any FPGA or MCU devices as well as dedicated power supplies, connectors etc.

Sheet Title FPGA, LEDs and SRAM Memory		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35			
Size: A4	Assy: D-820-0031	Revision:02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 7 of 23	
File: DEVICES.SchDoc			

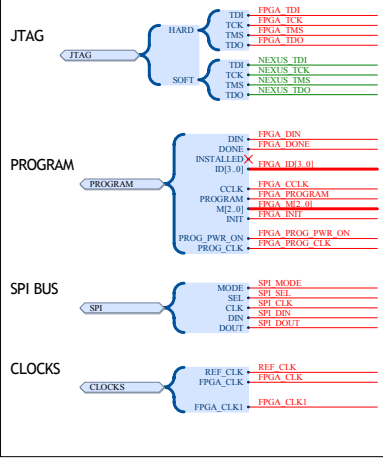
STATUS_LED 1 2 FPGA_DONE N16



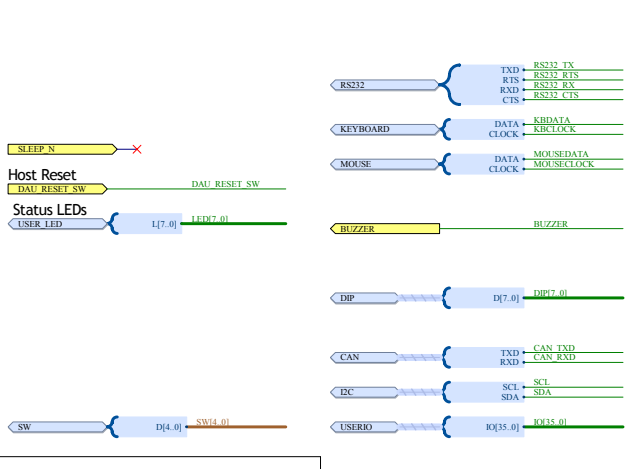
To permit DCI (terminated) inputs, the following must be done on each Bank: Tie the VRN pin (in each bank) through 50R to 3V3. Tie the VRP pin (in each bank) through 50R to GND.

Pin Nets labeled "UNUSEDxx" are not used for any function, they are labeled for the purposes of FPGA pin swapping only.

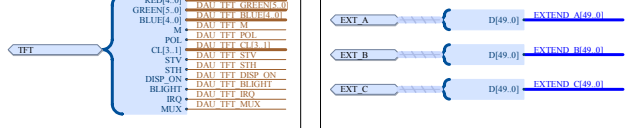
DAUGHTER BOARD I/O



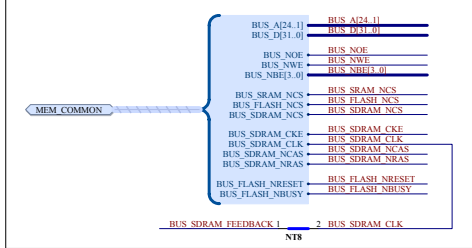
HOST PERIPHERALS



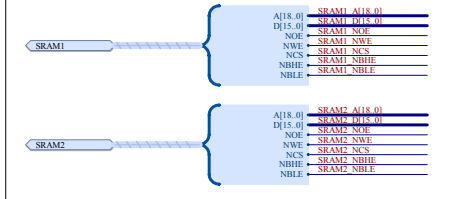
TFT LCD DISPLAY INTERFACE



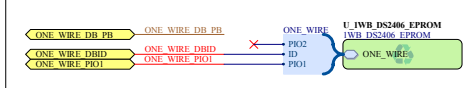
HOST MEMORY RESOURCES



DAUGHTER BOARD MEMORY RESOURCES

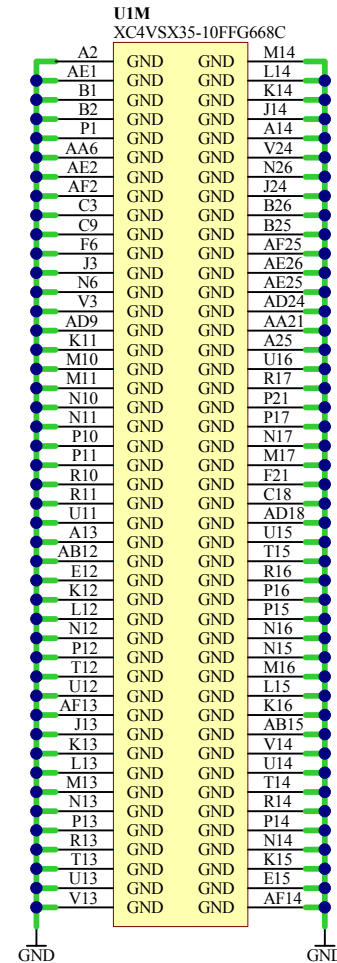
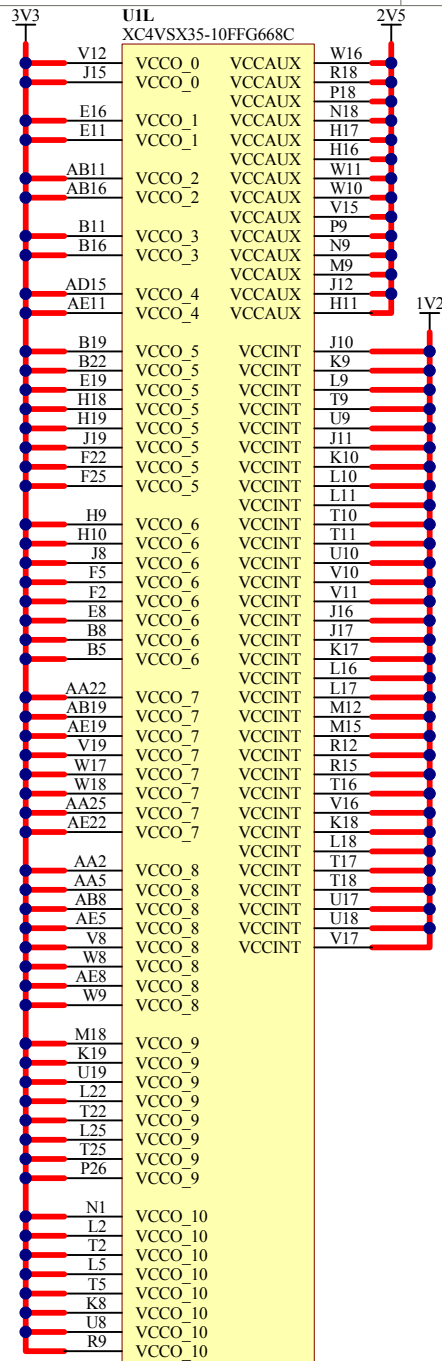
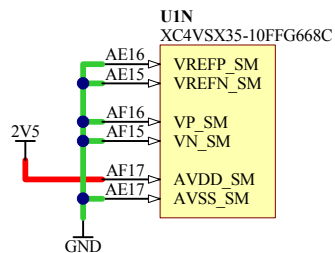
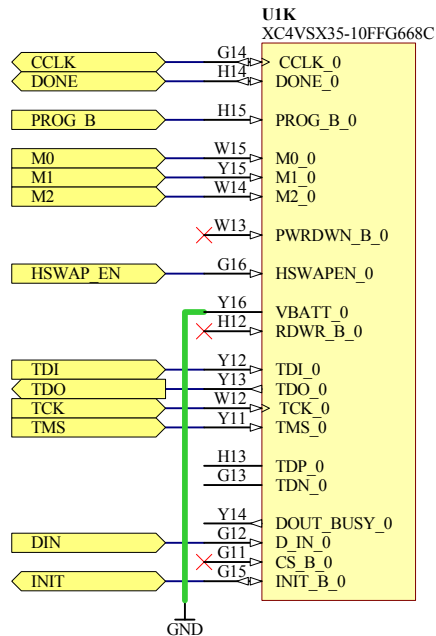


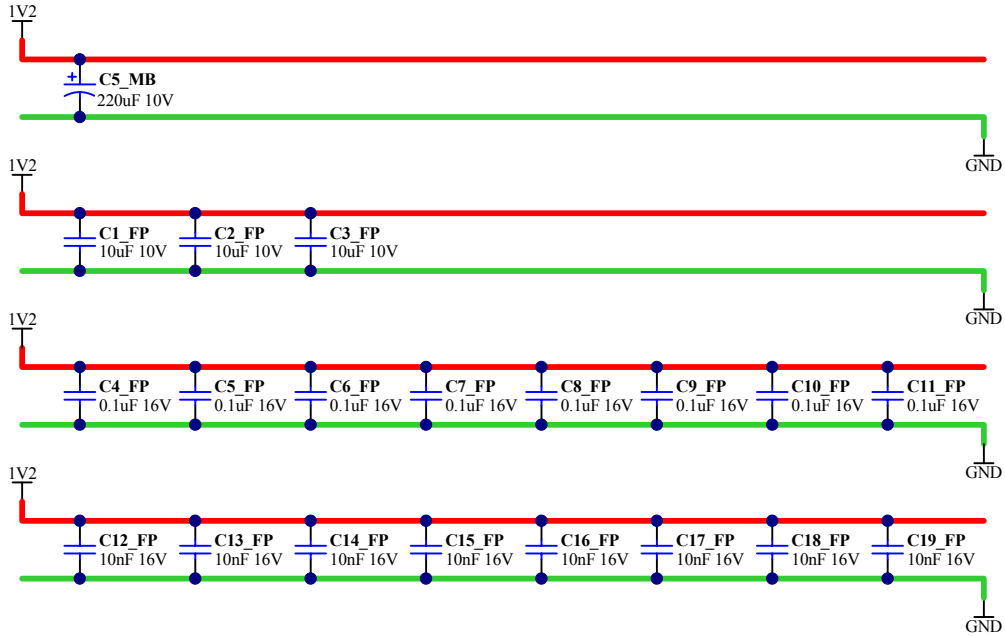
ONE-WIRE CONNECTIONS




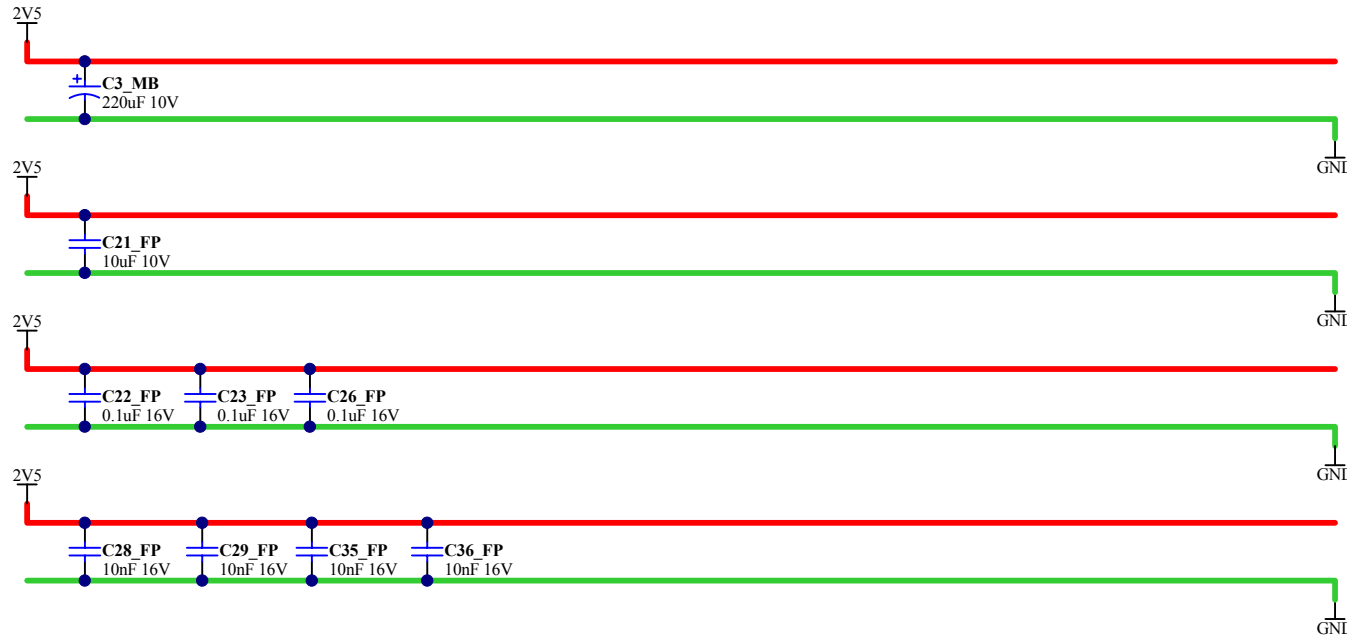
Pin lists for banks 5 through 16, including pin numbers, names, and functions for various components like SRAM, NEXUS, and I/O pins.




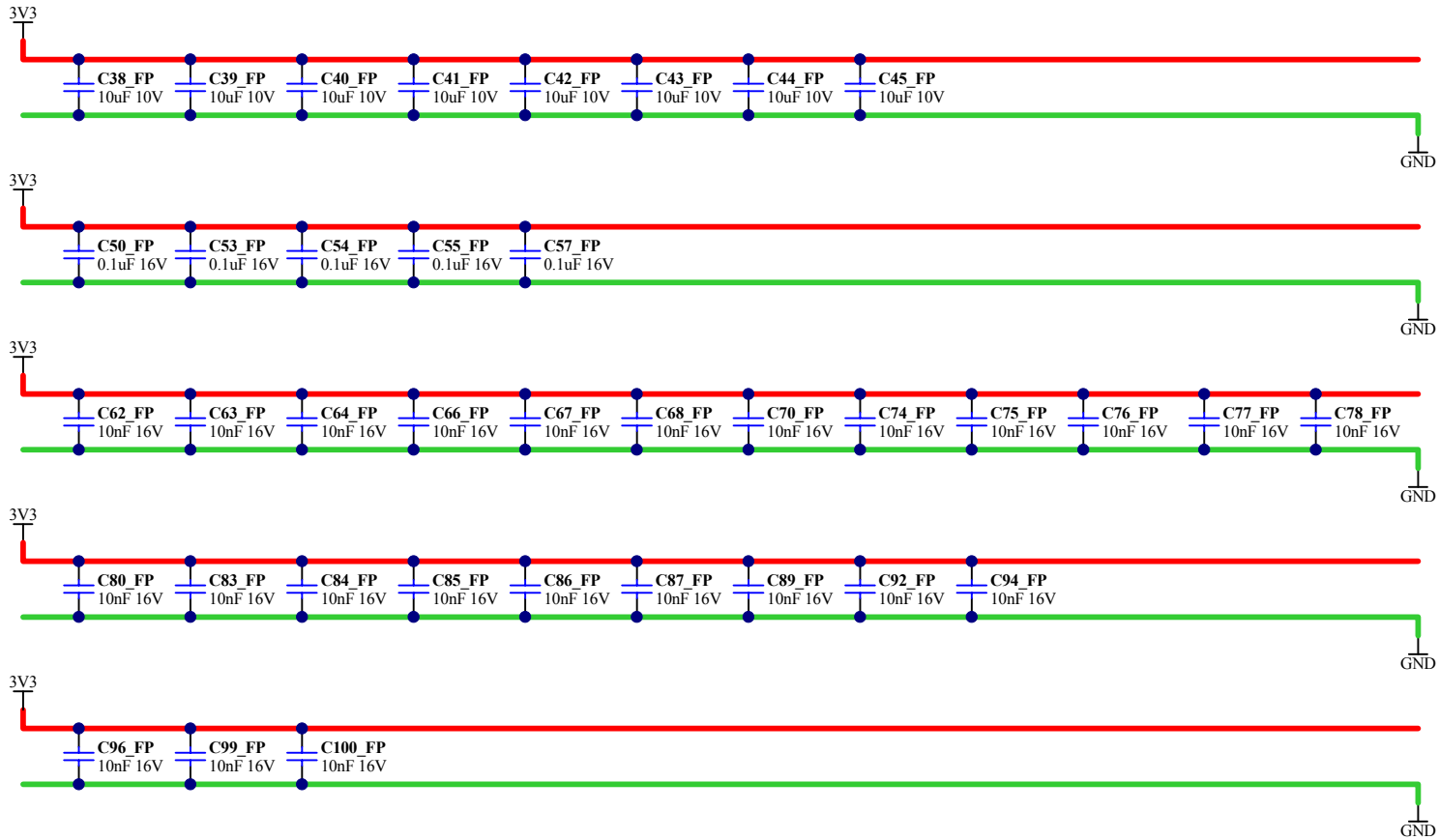




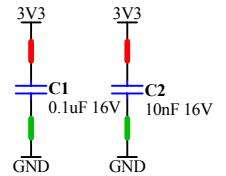
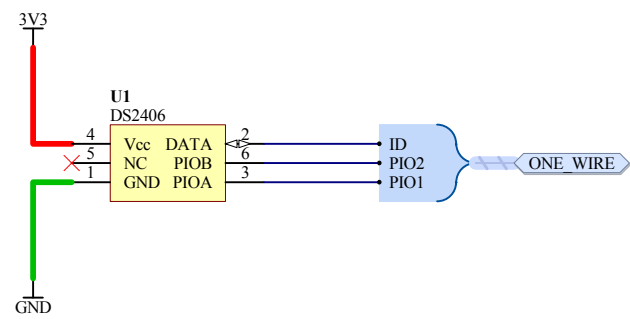
Sheet Title FPGA Bypass Capacitors for 1V2		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia		
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031			Revision:02
Date: 27/11/2008	Time: 4:51:04 PM			Sheet 10 of 23
File: Bypass FPGA 1V2.SCHDOC				




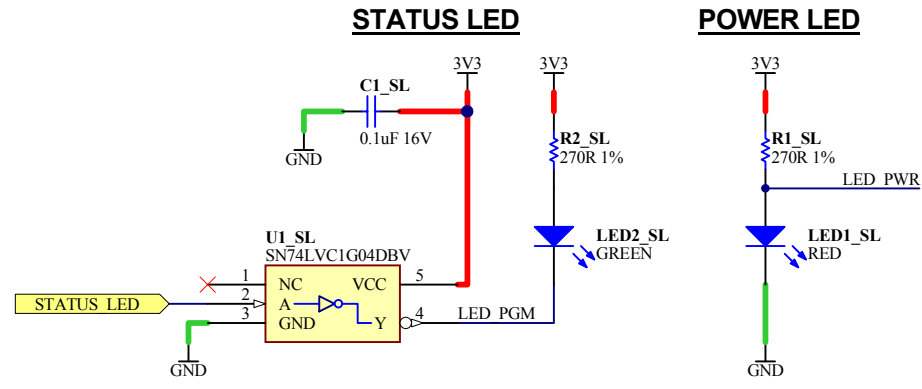
Sheet Title FPGA Bypass Capacitors for 2V5		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35			
Size: A4	Assy: D-820-0031	Revision:02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 11 of 23	
File: Bypass FPGA 2V5.SCHDOC			




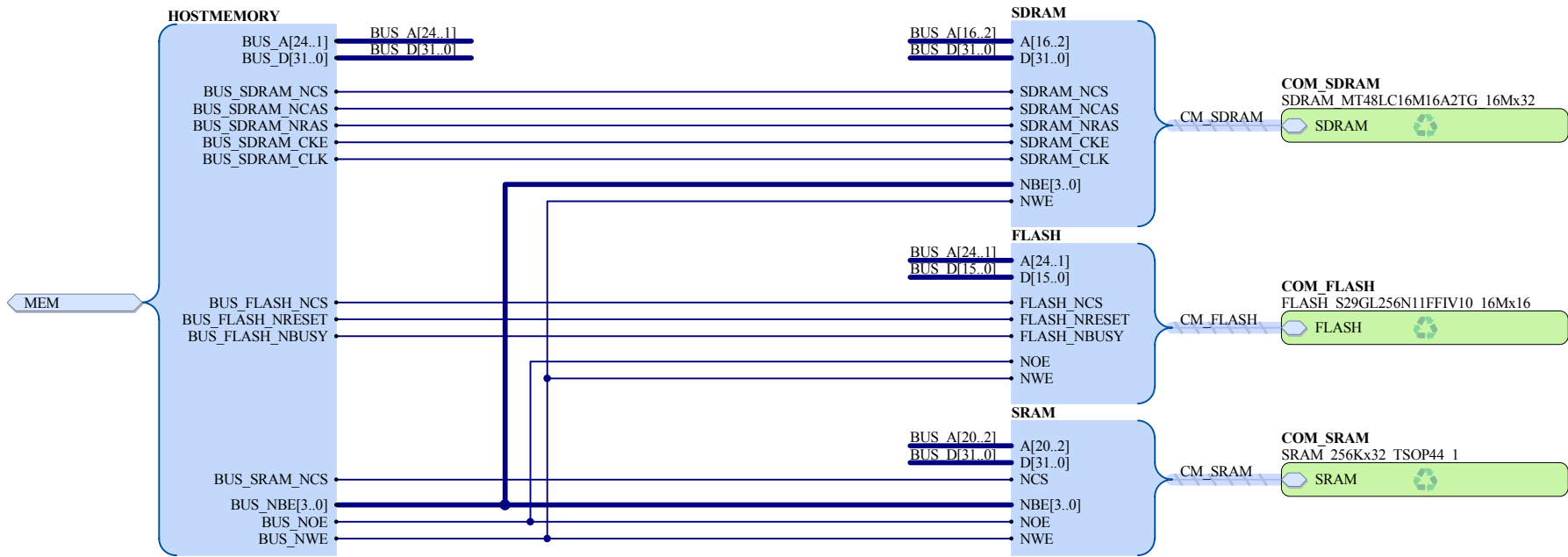
Sheet Title FPGA Bypass Capacitors for 3V3			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision:02		
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 12 of 23		
File: Bypass FPGA 3V3.SchDoc				



Sheet Title <i>1-Wire Bus ID</i>		<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title <i>DB46 - Virtex4 SX35</i>			
Size: A4	Assy: D-820-0031	Revision:02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 13 of 23	
File: 1WB_DS2406_EPROM.SchDoc			

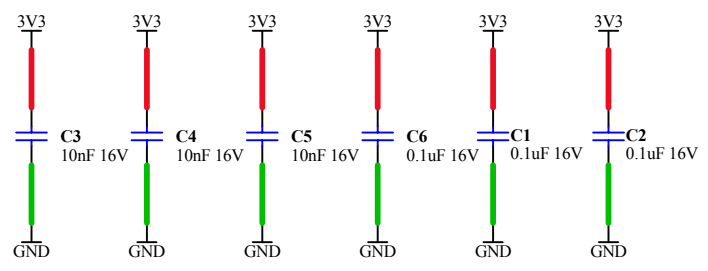
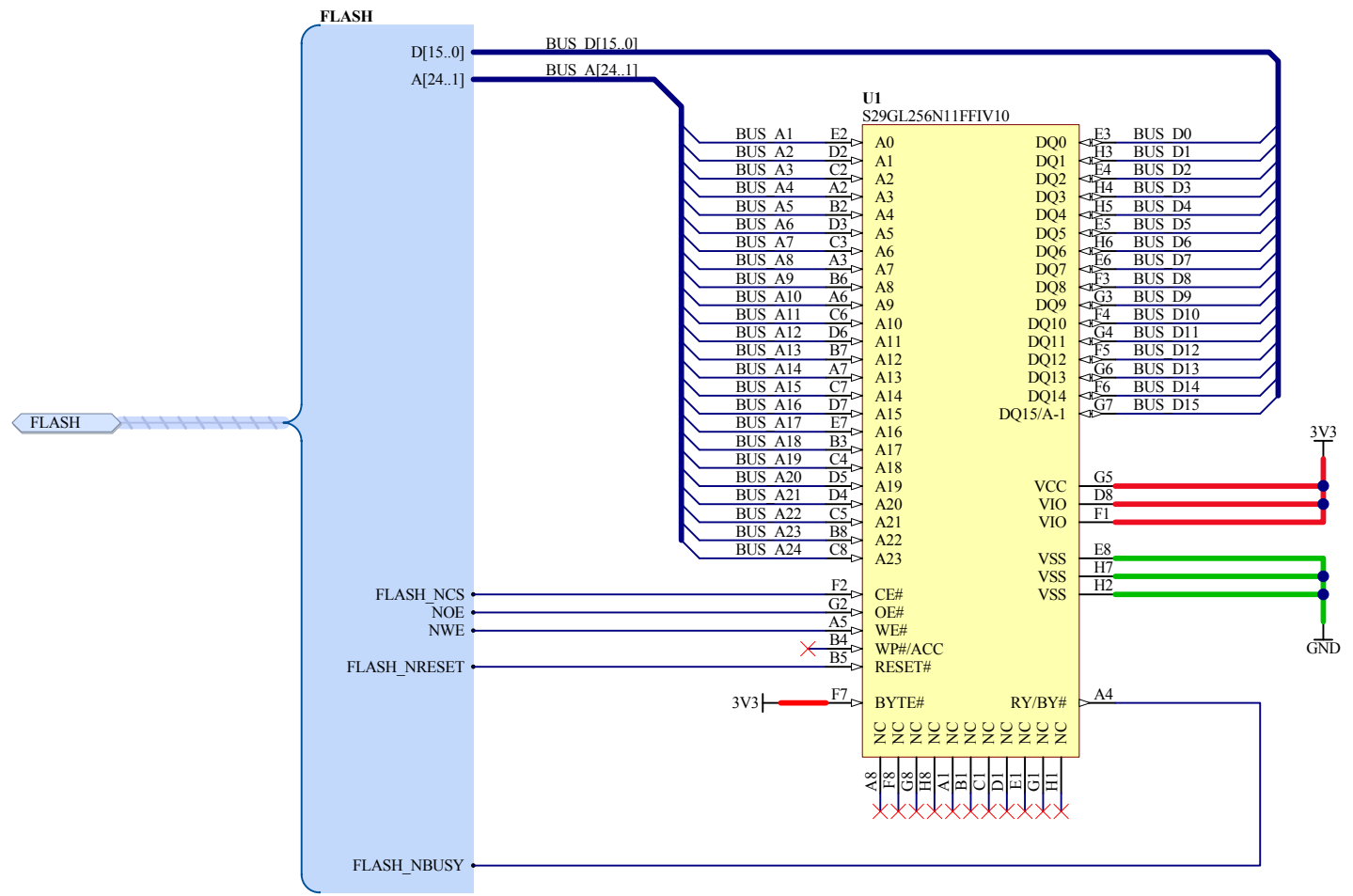


Sheet Title Daughter Board LEDs			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision:02		
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 14 of 23		
File: DB_LEDS.SchDoc				

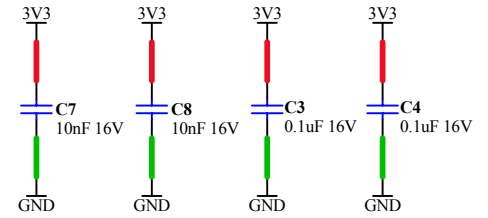
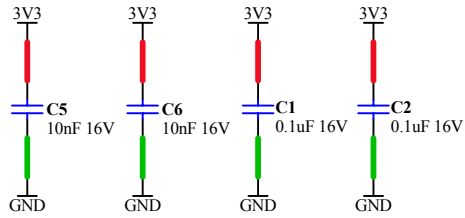
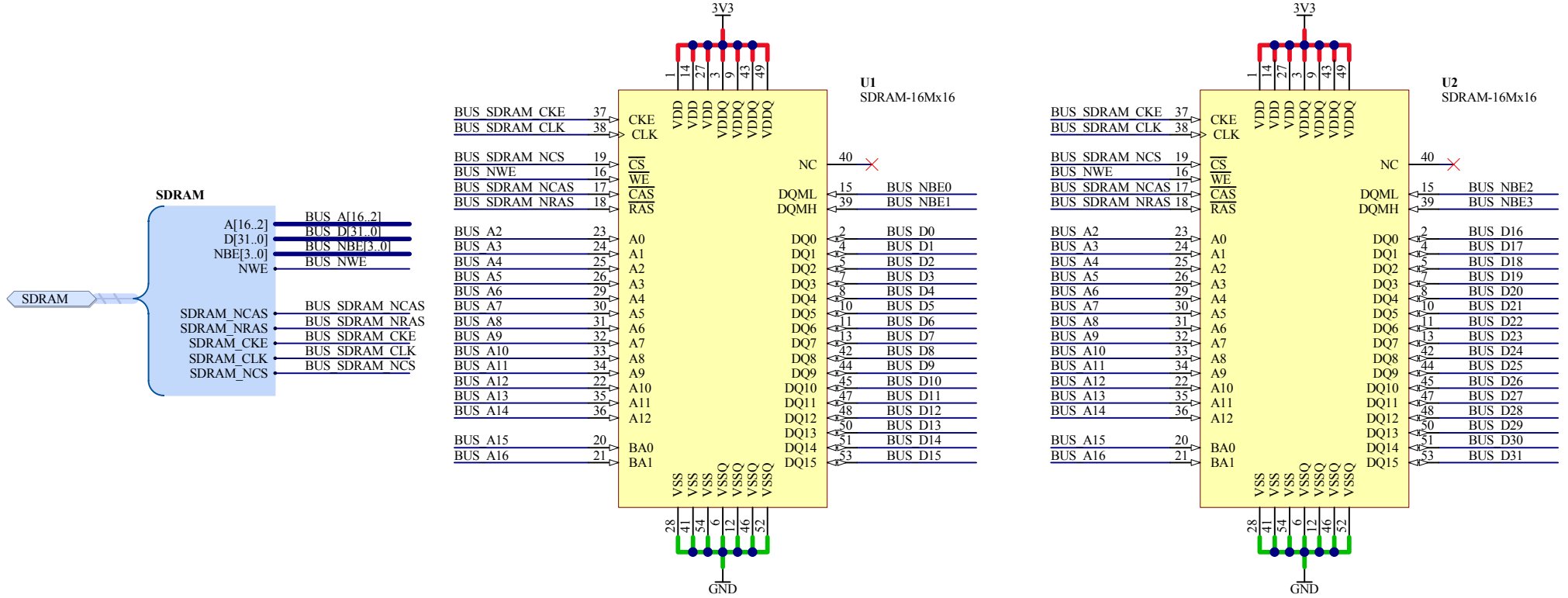


Common-Bus Memory Block
256K x 32-bit SRAM (1 MByte)
16M x 32-Bit SDRAM (64 MByte)
16M x 16-Bit Flash (32 MByte)

Sheet Title Common-Bus Memory Block			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision: 02		
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 15 of 23		
File: NB2_CommonMemory.SchDoc				

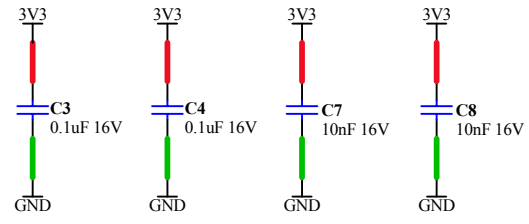
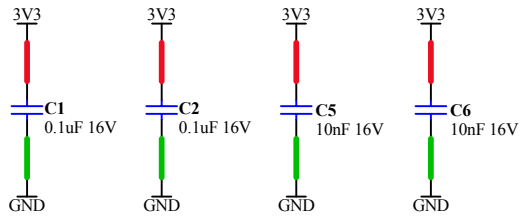
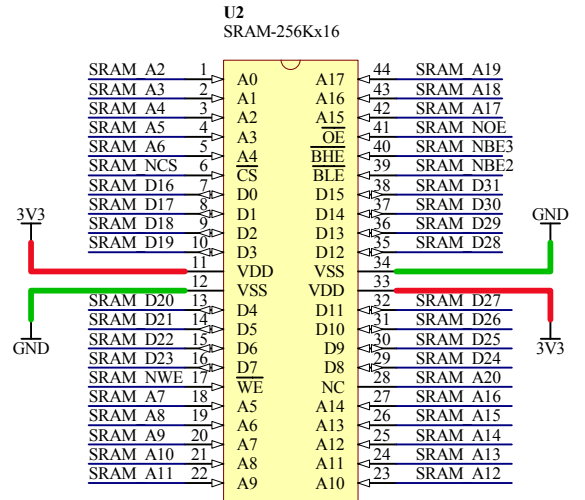
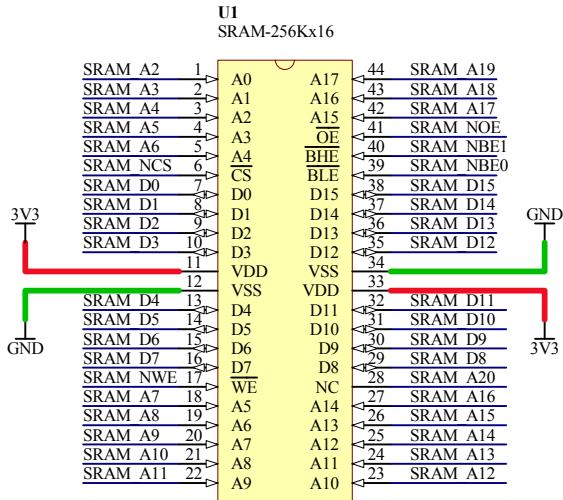
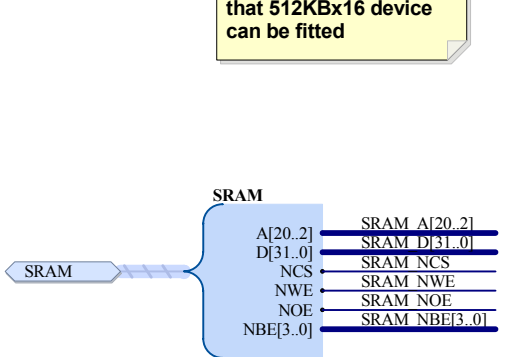


Sheet Title 16M x 16 Flash Memory (BGA)			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision: 02		
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 16 of 23		
File: FLASH_S29GL256N11FFIV10_16Mx16.SchDoc				



Sheet Title 16M x 32 SDRAM TSOP54 x 2			Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision: 02		
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 17 of 23		
File: SDRAM_MT48LC16M16A2TG_16Mx32.SchDoc				

A18 is connected so that 512KBx16 device can be fitted



Sheet Title **256K x 32 SRAM - TSOP44 x 2**
 Project Title **DB46 - Virtex4 SX35**
 Size: A4 Assy: D-820-0031 Revision: 02
 Date: 27/11/2008 Time: 4:51:04 PM Sheet 18 of 23
 File: SRAM 256Kx32 TSOP44 1.SchDoc

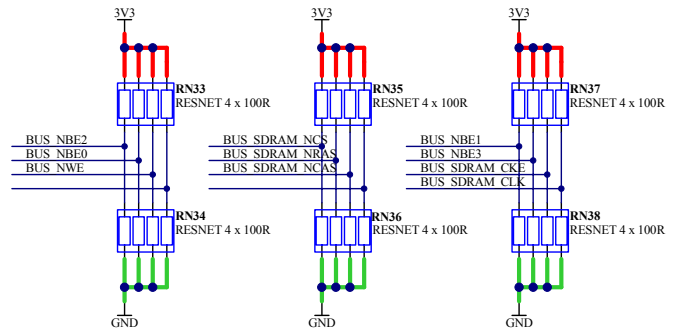
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 L3, 12A Rodborough Road
 Frenchs Forest
 NSW 2086
 Australia



HOSTMEMORY	
BUS_A[24..1]	BUS_D[31..0]
BUS_D[31..0]	BUS_D[31..0]
BUS_NBE[3..0]	BUS_NBE[3..0]
BUS_NOE	BUS_NOE
BUS_NWE	BUS_NWE
BUS_SDRAM_NCS	BUS_SDRAM_NCS
BUS_SDRAM_NCAS	BUS_SDRAM_NCAS
BUS_SDRAM_NRAS	BUS_SDRAM_NRAS
BUS_SDRAM_CKE	BUS_SDRAM_CKE
BUS_SDRAM_CLK	BUS_SDRAM_CLK
BUS_FLASH_NCS	BUS_FLASH_NCS
BUS_FLASH_NRESET	BUS_FLASH_NRESET
BUS_SRAM_NCS	BUS_SRAM_NCS
BUS_FLASH_NBUSY	

MEM

THESE SIGNALS TERMINATE AT THE SDRAM DEVICE



All devices using controlled impedance outputs from the source (ie. FPGA) should use 50 ohm (2 parallel 100 ohm resistors) termination.

The Flash should be located closest to the source (FPGA).
 The SRAM should be located next furthest from the source (FPGA).
 The SDRAM should be located next furthest from the source (FPGA).
 Terminations are to be located at the furthest distance from the source (FPGA).

Note that pins 5,6,7 and 8 of the following resnet "groups" are pin-swappable within that "group":

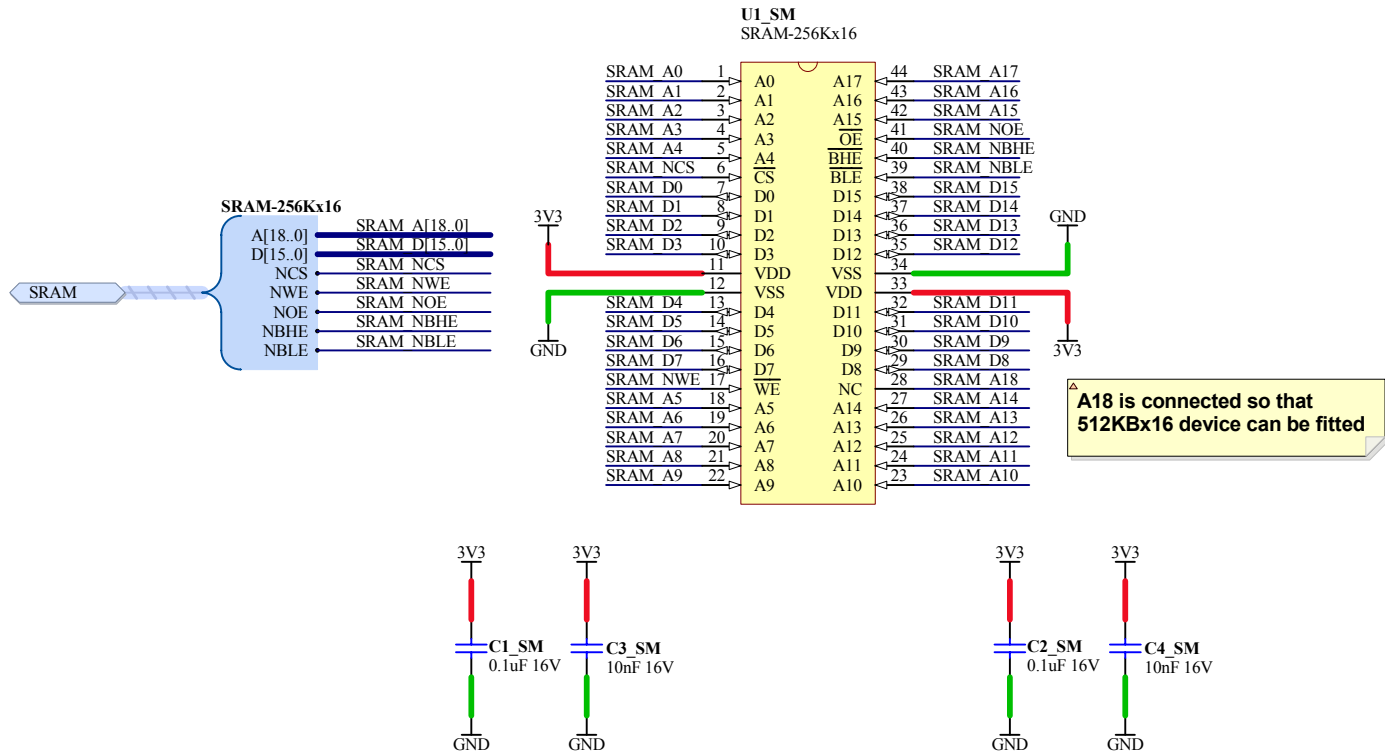
- all "power" resnets that terminate the FLASH-only signals (ie. RN1 and RN3).
- all "ground" resnets that terminate the FLASH-only signals (ie. RN2 and RN4).
- all "power" resnets that terminate the FLASH-SRAM-only signals (ie. RN5 and RN7).
- all "ground" resnets that terminate the FLASH-SRAM-only signals (ie. RN6 and RN8).
- all "power" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN9, RN11, RN13, RN15, RN17, RN19, RN21, RN23, RN25, RN27, RN29, RN31, RN33, RN35).
- all "ground" resnets that terminate the FLASH-SRAM-SDRAM signals (ie. RN10, RN12, RN14, RN16, RN18, RN20, RN22, RN24, RN26, RN28, RN30, RN32, RN34, RN36).

To remove any confusion by the PCB assembler, the following devices have been deleted entirely from the design: RN1 to RN16, and RN17 to RN32.

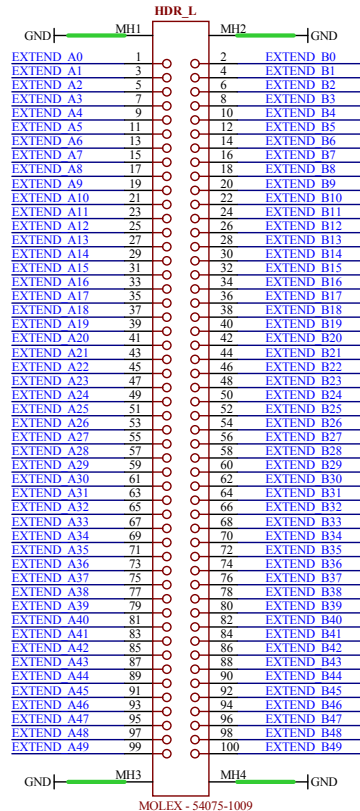
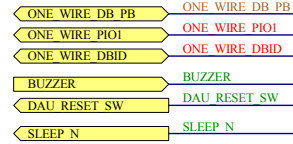
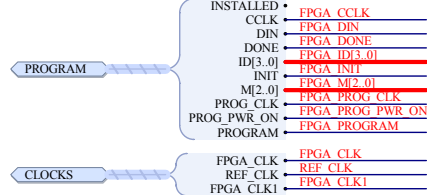
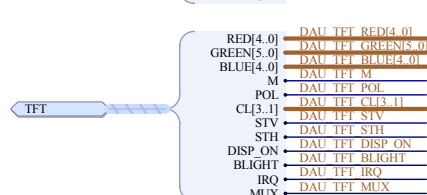
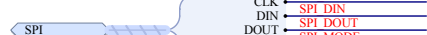
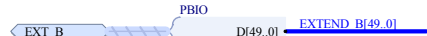
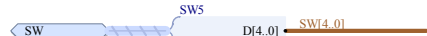
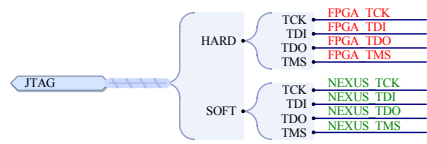
Note that high current (up to 1.25 Amps) is drawn from the 3V3 rail when all 19 pairs of resnets are loaded. The addition of up to 4.1 watts of heat was significantly warming the PCB.

Testing has confirmed that the loading of only 3 pairs of resnets (RN33/34, RN35/36 and RN37/38) provides good operation at speeds up to 96MHz. This consumes up to 0.20 amps, ie. up to 0.65 watts of heat.

The loading of the 3 pairs of resnets terminates only the output control signals from the FPGA to the SDRAM. The bidirectional data bus and address bus is not terminated. Signals that do not connect to the SDRAM (ie. signals to the slower flash and SRAM devices only) are also not terminated.



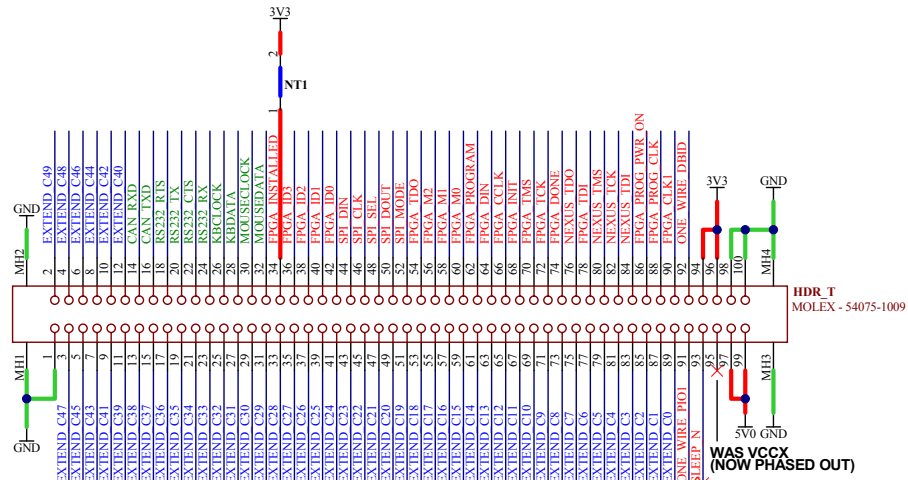
Sheet Title 256K x 16-Bit SRAM		Altium Limited L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35			
Size: A4	Assy: D-820-0031	Revision:02	
Date: 27/11/2008	Time: 4:51:04 PM	Sheet 20 of 23	
File: SRAM 256Kx16 TSOP44.SchDoc			



Red Connections are locked for NB1 compatibility. They are hardwired on the NB1 and therefore can NOT be changed.

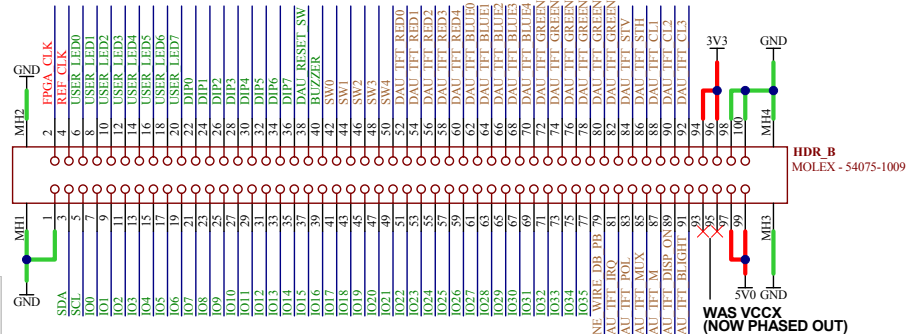
Green connections are I/O pins connected to NB1 compatible PCB resources on the mother board. These can be changed.

Blue connections are connected to the New NB2 compatible resources on the motherboard. These can be changed.



Note that the signal ONE_WIRE_DBID was previously called FPGA_CLK2.

This signal was included in NB1 design, but never used. Hence it has now been reallocated.



1

2

3

4

A

A

B

B

C

C

D

D

U_MOUNTS
DB MOUNTS




PCB1
DB46 Blank PCB
Printed Circuit Board (Bare)

Fiducial Alignment Components

FD1 Fiducial - Round FD2 Fiducial - Round



Sheet Title DB46 Hardware Kit			<i>Altium Limited</i> L3, 12A Rodborough Road Frenchs Forest NSW 2086 Australia	
Project Title DB46 - Virtex4 SX35				
Size: A4	Assy: D-820-0031	Revision:02		
Date: 27/11/2008	Time: 4:51:05 PM	Sheet 22 of 23		
File: DB46 Hardware Kit.SchDoc				

1

2

3

4

1

2

3

4

A

A

B

B


C

C

D

D


MH1
MOUNTING HOLE 3MM



MH2
MOUNTING HOLE 3MM



MH3
MOUNTING HOLE 3MM




Altium Logo Top1



Altium Logo Bot1



Sheet Title <i>Mounts, Logo & Label</i>			<i>Altium Limited</i> <i>L3, 12A Rodborough Road</i> <i>Frenchs Forest</i> <i>NSW 2086</i> <i>Australia</i>	
Project Title <i>DB46 - Virtex4 SX35</i>				
Size: A4	Assy: D-820-0031	Revision: 02		
Date: 27/11/2008	Time: 4:51:05 PM	Sheet 23 of 23		
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