



Constraint File Reference

Summary

This document describes the constraint file syntax, including a list of FPGA-specific constraint definitions.

Technical Reference
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FPGA designs are captured in the Altium Designer design environment as schematics and VHDL files. Implementation information, such as device pin allocations and pin electrical properties are not stored in these source files, they are stored in separate constraint files. One or more constraint files can be mapped to an FPGA project by adding them to a project Configuration.

 Refer to the article, [Design Portability, Configurations and Constraints](#) for a detailed description of the role of configurations and constraints.

Defining Constraints

Constraints are normally defined in constraint files, using the constraint editor. To add a new constraint file to a project right-click on the project name, then from the **Add New to Project** submenu select **Constraint File**. Constraints can be defined by typing them in, or by adding them using the menu options available in the constraint file editor **Design** menu.

Multiple constraint files can be used, allowing you to separate constraints by their type. For example, you can add design-specific constraints (such as specifying a net to be a clock) in one constraint file, and implementation type constraints (such as pin allocations) in a second constraint file.

Constraint files are mapped to an FPGA design by defining a Configuration, this can be done by right-clicking on the project filename in the panel and selecting **Configuration Manager**. Multiple constraint files can be enabled in a configuration. When an FPGA design is implemented in a device you select a project/configuration combination, allowing the system to map the design to its implementation. By defining multiple configurations you can easily re-target a design from one device to another.

Certain constraints can also be defined on the source schematic files. Be aware that these can lock the design down, for example specifying the target device on the schematic would prevent you from implementing that design on another device until you edit that parameter. Constraints that would be appropriate to define on the schematic include circuit-specific constraints, such as defining a net to be a clock.

Refer to the article mentioned above for more details on configurations and constraints.

Constraint File Basics

Each line in a constraint file is referred to as a constraint group, since it applies one or more constraint requirements to an entity in the design. The following examples show a variety of different constraint groups.

Example 1

```
Record=Constraint | TargetKind=Part | TargetId=XC2S300E-6PQ208C
```

This constraint targets the part (or FPGA component), in this case specifying the type as XC2S300E-6PQ208C. Note that this device must be supported by the system, select the **Design » Add/Modify Constraint » Part** menu item to display the *Choose Physical Device* dialog. This dialog displays all devices supported by the system. This constraint group should only appear once in any configuration.

Example 2

```
Record=Constraint | TargetKind=Port | TargetId=VGA_VSYN | FPGA_PINNUM=P134
```

This constraint group targets the net connected to port VGA_VSYN, specifying that it be connected to FPGA pin number P134.

Example 3

```
Record=Constraint | TargetKind=Port | TargetId=LCD_E | FPGA_PINNUM=P82 | FPGA_IOSTANDARD=LVTTL33 |  
FPGA_SLEW=SLOW | FPGA_DRIVE=12mA
```

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This constraint group targets the net connected to the port LCD_E, specifying that it be connected to FPGA pin number P82, have an I/O standard of LVTTTL33, a slew setting of slow, and a drive current of 12 mA.

Example 4

```
Record=Constraint | TargetKind=Port | TargetId=VGA_R[1..0] | FPGA_PINNUM=P145,P141
```

This constraint group targets both the nets in the bus connected to the port VGA_R[1..0], specifying that the bus element 1 connect to pin P145, and bus element 0 connect to pin P141.

Importing Constraints from Place and Route

Design constraint detail can also be assigned and generated by the vendor place and route tools. For example, if you have not constrained a port in the FPGA design to a device pin, the place and route tools will do this. Use the options in the **Design » Import Pin File** menu in the constraint file editor to import constraints defined by the place and route software.

Constraint Definitions

Record

Summary Defines purpose of entry in the constraint file.

Values FileHeader, Constraint

TargetKind

Summary Defines what this record in the constraint file applies to.

Values Part, PCB, Port, Net

TargetId

Summary Name of object being targeted by the constraint record.

Values Name of port on top sheet of schematic, device part number, name of PCB

Id

Summary FileHeader constraint, specifies the type and version of constraint file.

Values varied, eg DXP Constraints v1.0

FPGA-Specific Constraint Definitions

These constraints must be used in conjunction with the device vendor's component specifications to ensure that a particular constraint is supported in that device.

FPGA_CLOCK

Summary States that the top level port of the target technology should use a high speed resource.

Values True, False

TargetKind Port

Define as Constraint file entry, Port Parameter

Vendors Actel, Altera, Xilinx

FPGA_CLOCK_DUTY_CYCLE

Summary Sets the duty cycle of the clock.

Values Percentage

TargetKind Port

Define as Constraint file entry, Port Parameter

Vendors Actel, Altera, Xilinx

FPGA_CLOCK_FREQUENCY

Summary	Sets the desired frequency of the clock, the place and route tool will attempt to achieve this frequency (but they do not guarantee that it will).
Values	Number followed by units. ie 50 Mhz etc
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Actel, Altera, Lattice, Xilinx

FPGA_CLOCK_PIN

Summary	States that the top level port is connected to a reserved clock pin on the target device.
Values	True, False
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Xilinx

FPGA_DEVICE

Summary	Specifies the target device
Values	Device specification, as detailed in the Device field of the <i>Choose Physical Device</i> dialog.
TargetKind	Part
Define as	Constraint file entry, Sheet Parameter
Vendors	Altera, Lattice, Xilinx

FPGA_DRIVE

Summary	specifies the current strength of a pin in the target device, and may be applied to ports in the top level entity.
Values	Drive current (eg 12mA)
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Altera, Lattice, Xilinx

FPGA_GLOBAL

Summary	States that the signal should be kept and use a high speed resource.
Values	True, False
TargetKind	Net
Define as	Parameter in Parameter Set object attached to net
Vendors	Altera, Xilinx

FPGA_INHIBIT_BUFFER

Summary	No I/O buffers are inserted at the pin
Values	True, False
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Xilinx

FPGA_IOSTANDARD

Summary	Specifies the pin IO standard in the target device, and may be applied to ports in the top level entity.
Values	Refer to vendor device documentation
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Altera, Lattice, Xilinx

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FPGA_KEEP

Summary	Prevents a particular signal from being optimized.
Values	True, False
TargetKind	Net
Define as	Port Parameter
Vendors	Altera, Xilinx

FPGA_NOCLOCK

Summary	Prevents the synthesizer from placing a clock buffer. The synthesizer has the ability to infer clock buffers and add them in automatically.
Values	True, False
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Altera, Xilinx

FPGA_PCI_CLAMP

Summary	Enables Peripheral Component Interconnect (PCI) compatibility for a pin.
Values	True, False
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendor	Altera(Cyclone/Stratix)

FPGA_PINNUM

Summary	Specifies the pinout in the target device, and may be applied to ports in the top level entity.
Values	device pin number, in the format required by the vendor tools
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Actel, Altera, Lattice, Xilinx

FPGA_PULLDOWN

Summary	Adds a pulldown resistor to an input/output port.
Values	True, False
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Xilinx

FPGA_PULLUP

Summary	Adds a pullup resistor to an input/output port.
Values	True, False
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Altera, Xilinx

FPGA_RESERVE_PIN

Summary	Ensures that the place and route tools do not assign this particular pin to a port of your design.
Values	Number of pin to be reserved
TargetKind	Pin
Define as	Constraint file entry
Vendors	Actel, Altera, Xilinx

FPGA_SLEW

Summary	Specifies the slew standard in the target device, and may be applied to ports in the top level entity.
Values	Refer to vendor device documentation
TargetKind	Port
Define as	Constraint file entry, Port Parameter
Vendors	Actel, Altera, Lattice, Xilinx

Revision History

Date	Version No.	Revision
18-Dec-2003	1.0	New product release
15-Jun-2005	1.1	Updated for Altium Designer SP4
04-Mar-2008	2.0	Updated for Altium Designer Summer 08

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