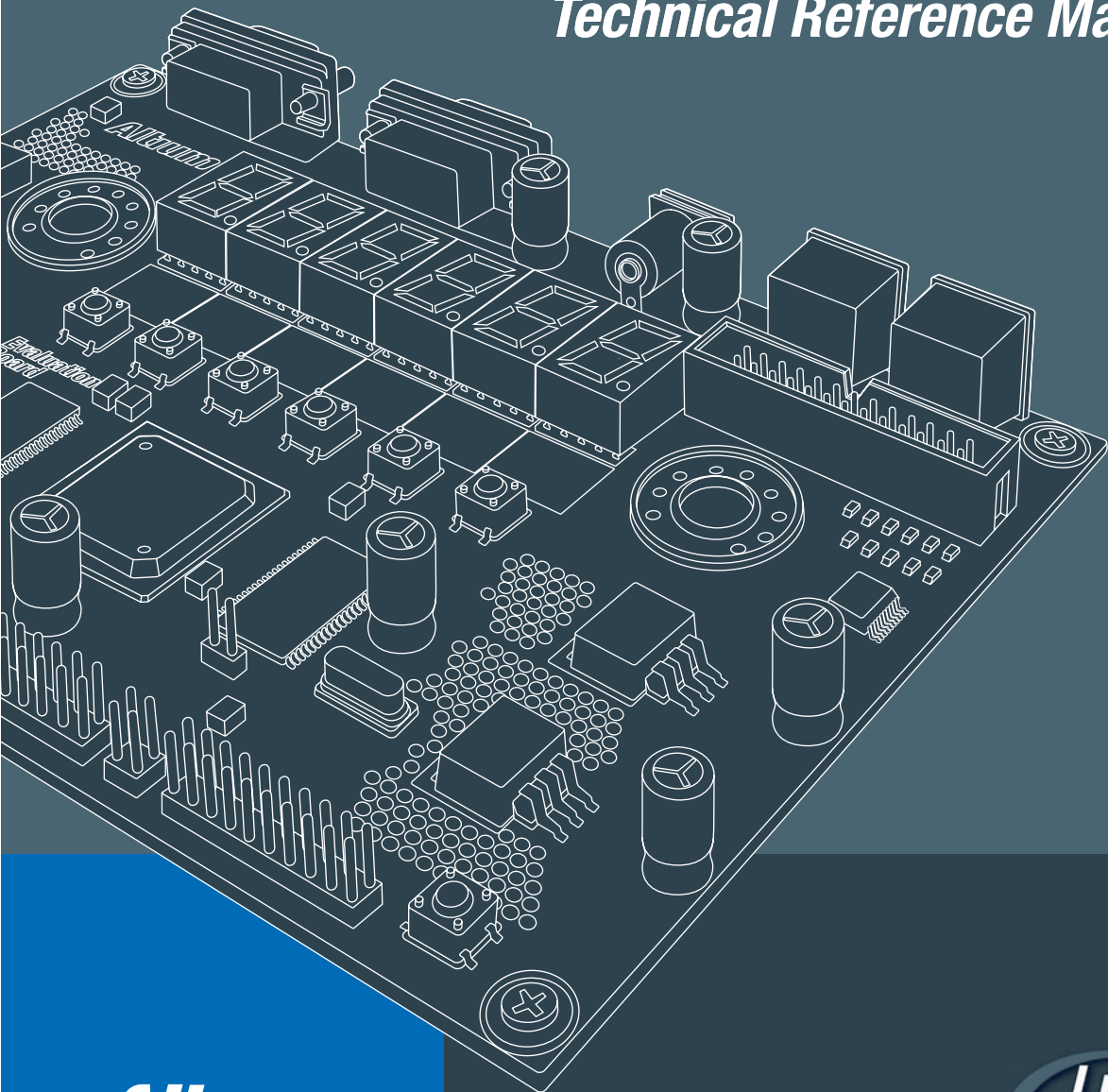


LiveDesign Evaluation Board

Technical Reference Manual





LiveDesign Evaluation Board Technical Reference Manual

Technical reference manual for
Altium's LiveDesign Evaluation Boards



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About This Manual

This document describes the board level operations of Altium's LiveDesign Evaluation Boards.

Revision History

Date	Version No.	Revision
22-Sep-04	1.0	New product release

Notational Conventions

This document uses the following conventions.

- Field Programmable Gate Arrays (FPGA) or Complex Programmable Logic Devices (CPLD) may be collectively referred to as FPGA or CPLD
- Interactive instructions are shown in a bold typeface, for example:

Continue

View » Devices

Information About Cautions

This manual may contain cautions.



Caution statements look like this.

A caution statement describes a situation that could potentially damage your software, hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

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Introduction to the LiveDesign Evaluation Board

This chapter outlines the key features and capabilities of the LiveDesign Evaluation Board.

The LiveDesign Evaluation Board, in conjunction with an evaluation license of Altium's DXP 2004 PC-based development software, provides you with the ability to evaluate and fully experience the benefits of LiveDesign allowing for the rapid and interactive implementation and debugging of FPGA designs.

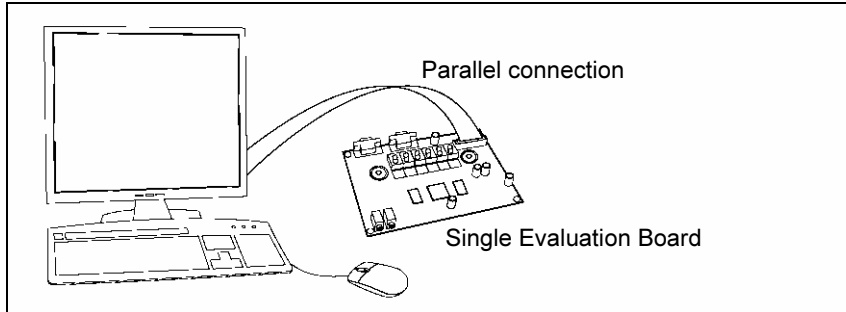


Figure 1. PC connected to the LiveDesign Evaluation Board

Key Features of the LiveDesign Evaluation Board

The LiveDesign Evaluation Boards have the following features:

- On-board FPGA Device*
- Dual 256Kx16 BIT FPGA configurable High Speed Static RAM
- Audio System, Delta Sigma stereo DAC with user-adjustable corner frequency
- Dual (stereo) miniature speakers with volume control
- Audio Line Out and Headphone 2.5mm jacks with volume control
- 6 Digit 7-Segment LED display
- Fixed 50mHz clock
- RS232 Serial Port
- VGA Port
- PS2 Mini DIN Mouse Port
- PS2 Mini DIN PC Keyboard Port
- 8-way DIP switch
- LED array, 8 LEDs
- Dual 20 pin I/O expansion headers with power supply selection links
- User-defined TEST/RESET button

* Various LiveDesign Evaluation Boards are available targeting different FPGA devices, such as Xilinx Spartan-3 and Altera Cyclone. Visit www.altium.com/dxpcentral for a full listing of LiveDesign Evaluation Boards currently available.

Functional Overview of the LiveDesign Evaluation Board

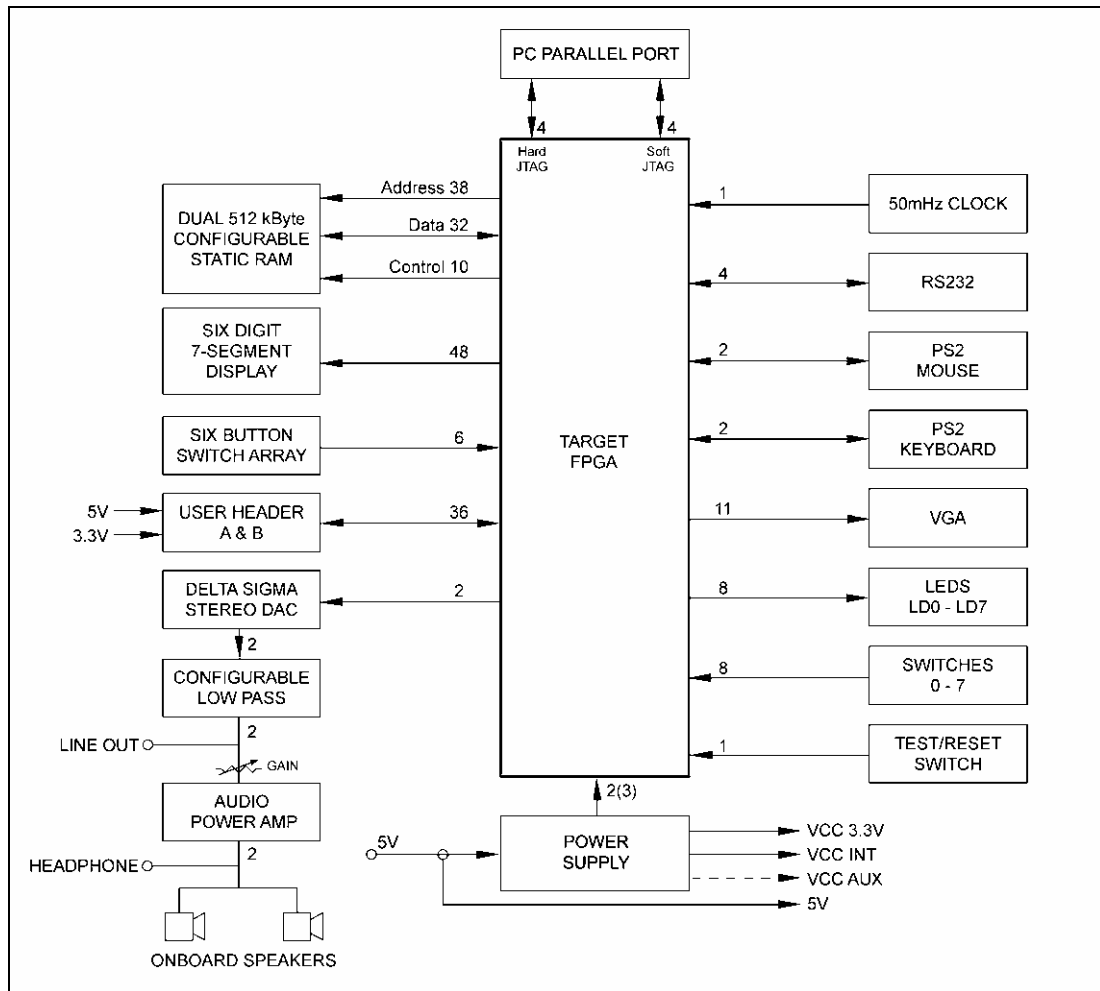


Figure 2. A block diagram of the LiveDesign Evaluation Board configuration

Getting Started

This section gives step-by-step instructions on connecting the LiveDesign Evaluation Board to your PC and testing the PC to the LiveDesign Evaluation Board connectivity. It is recommended that this section be thoroughly read before beginning the installation and setup process.



CAUTION: Observe standard antistatic procedures when handling the board. Always power down when making changes to the configuration of the board, for example, when adding or removing plug-in devices to the LiveDesign Evaluation Board expansion headers.

What's in the box

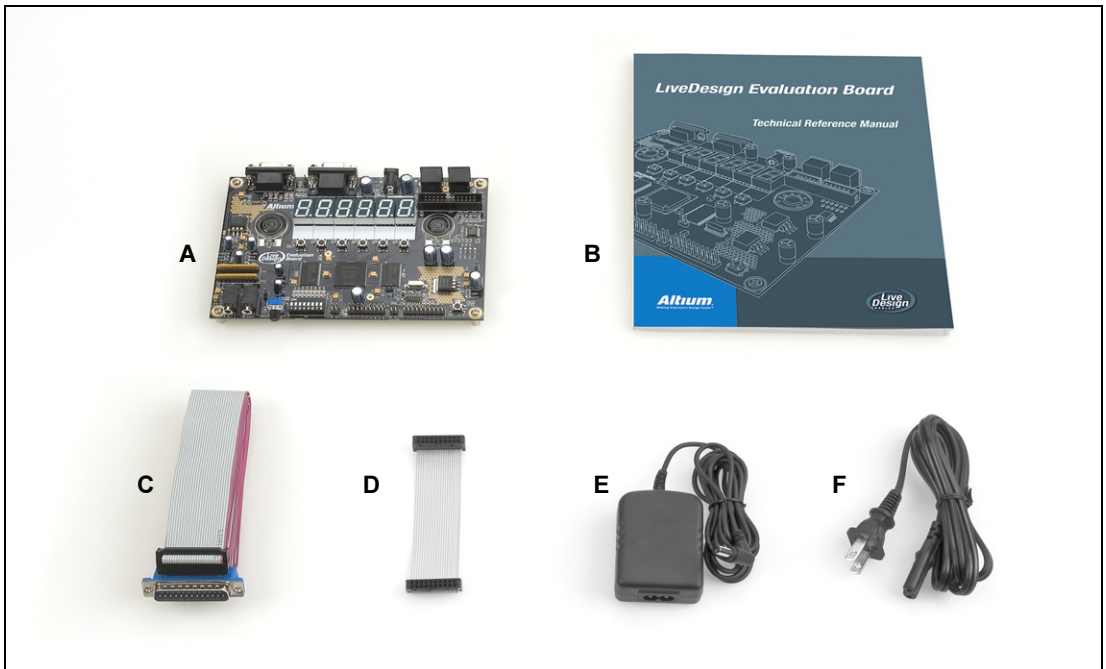


Figure 3. LiveDesign Evaluation Board package contents

- A – LiveDesign Evaluation Board
- B – LiveDesign Evaluation Board Technical Reference Manual
- C – Parallel cable (26 way IDC - DB25)
- D – User header cable (20 way IDC - 20 way IDC) (x2)
- E – Power Supply
- F – Power Supply Cord

If any of these components are missing or appear damaged, please contact your nearest Altium Sales & Support Center or Reseller.

System requirements

Before installing the software, please ensure that your computer meets the minimum system requirements listed below.

Recommended system

To get the most from your Altium design software, we recommend a PC with the following specifications:

- Windows XP (Professional or Home) or Windows 2000 Professional
- 2 GHz Pentium 4 processor or equivalent
- 1 GB RAM
- 2 GB hard disk space (Install + User Files)
- Dual monitors with 1280x1024 screen resolution
- 32-bit color, 64 MB graphics card
- Parallel port.

Minimum requirements

The following computer specifications are the minimum needed to get adequate performance from your design software:

- Windows XP (Professional or Home) or Windows 2000 Professional
- 1 GHz processor
- 512 MB RAM
- 2 GB hard disk space (Install + User Files)
- Main monitor 1280x1024 screen resolution
- Strongly recommended: second monitor with minimum 1024x768 screen resolution
- 32-bit color, 32 MB graphics card
- Parallel port.

Altium design software

To install your Altium design software, you will need approximately 1GB of free disk space. To begin the installation process, simply insert the Software Installation CD into your computer's CD ROM drive. The Installation Wizard will automatically start and guide you through the installation process.

If the Installation Wizard does not start automatically, please run Setup.exe located in the \Setup directory of the CD.

The first time you run the software, you will be required to activate it. To do this, use the Active License options in the DXP License Management page.

Once the installation of the software is complete, you should install the necessary FPGA vendor tools – if not already present – and then connect the LiveDesign Evaluation Board to your PC before starting the design system.

Refer to the *LiveDesign Evaluation Kit Quickstart Guide* for detailed step by step instructions on the software installation and license activation process.

Important note on FPGA vendor tools

To place and route the FPGA design for the target FPGA device on the LiveDesign Evaluation Board, FPGA vendor tools are used. The FPGA vendor tools ARE NOT supplied with the system and must be sourced independently.

Before you can download a design to the LiveDesign Evaluation Board, you must have the appropriate vendor tools installed on your computer.

Each LiveDesign Evaluation Board comes supplied with a target FPGA supported by the appropriate vendor's freely-downloadable tools available on the web, as well as by the commercial versions of these tools.

More information on the vendor tools for the supported FPGA devices can be found on the FPGA vendor's website. For the latest information on vendor tools supported by Altium's software, as well as links to the appropriate websites, visit www.altium.com/dxpcentral.

Please note that Altium does not provide technical support for FPGA vendor tools. For information on installing these tools, please refer to the information provided by the FPGA vendors.

Setting up the LiveDesign Evaluation Board

The LiveDesign Evaluation Board gets connected to your PC via the computer's parallel port. The picture in Figure 4 shows an image of the LiveDesign Evaluation Board highlighting the location of the main components addressed during installation.

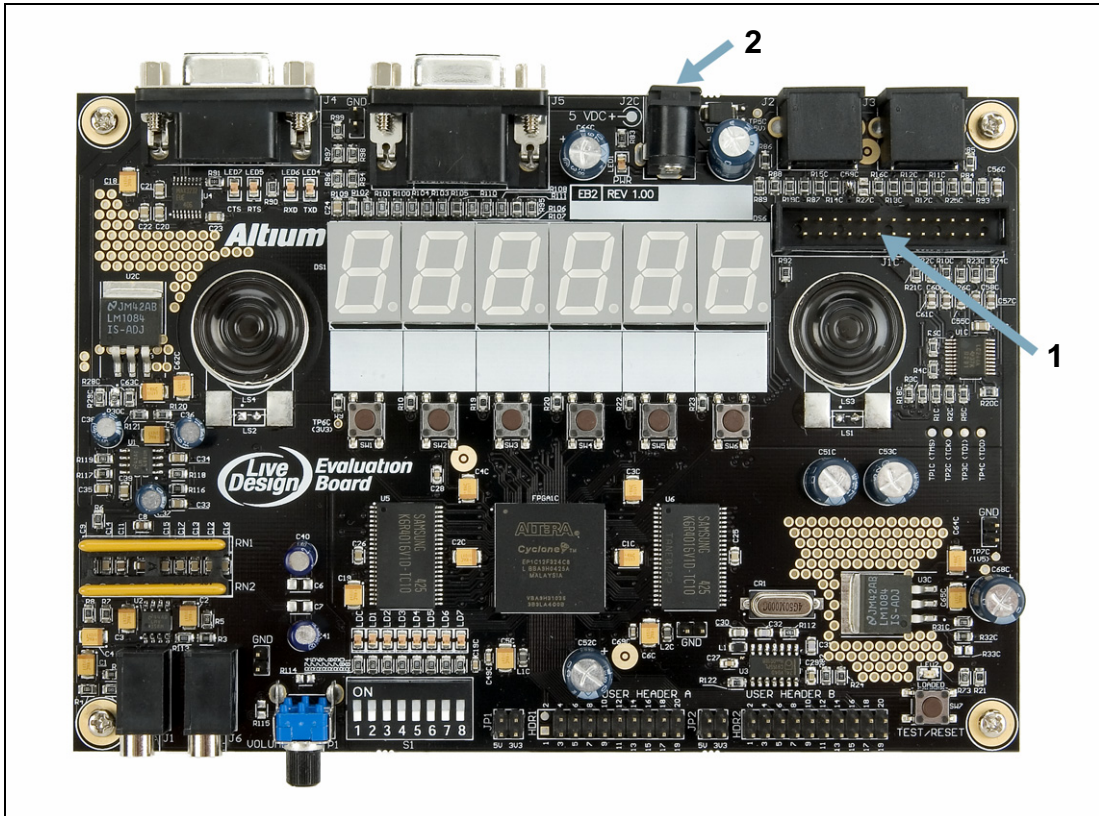


Figure 4. The LiveDesign Evaluation Board, 1 = Parallel header socket 2 = Power supply socket

To start-up the LiveDesign Evaluation Board complete the following steps:

1. Connect the LiveDesign Evaluation Board to your PC using the parallel cable supplied, via the parallel header socket, pointed out in Figure 4.
2. Power the board using the 5 volt DC power supply via the power supply socket pointed out in Figure 4. Once powered the power indicator LED will illuminate.

Testing the PC to LiveDesign Evaluation Board connection

Once you have connected the LiveDesign Evaluation Board to your PC, you should check that the system software can connect to the LiveDesign Evaluation Board.

To do this, follow the steps below.

1. Start your Altium design system by selecting the **DXP 2004** icon from the Windows **Start** menu.
2. The first time the system is run with a LiveDesign Evaluation Board connected, it will build a cache of supported programmable devices. A progress dialog will appear on screen during this process. Building the cache can take several minutes, depending on the speed of your computer. This only needs to be done once.

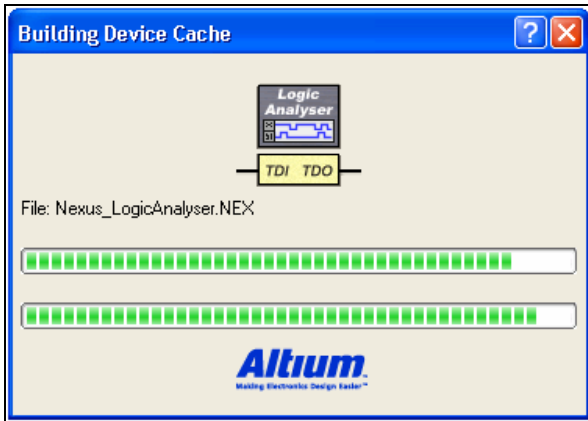


Figure 5. Device cache progress report

Once the system has started, you will be presented with the DXP 2004 Home page, as pointed out in Figure 6, which provides a jump point to many of the features offered by the system.

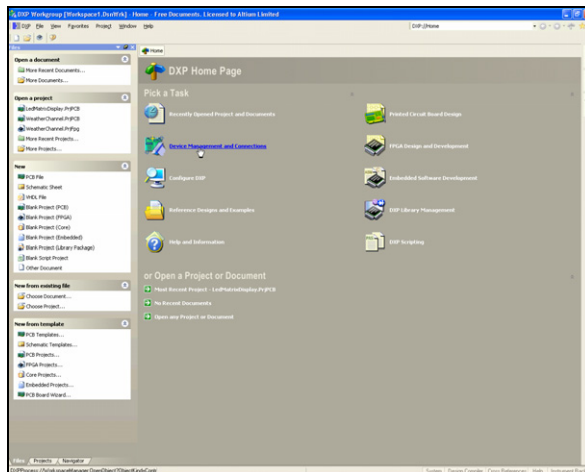


Figure 6. The DXP 2004 Home page

3. Click on the **Device Management and Connections** icon.

This will open the **Devices** view. Alternatively, you can select **View » Devices** from the menus.

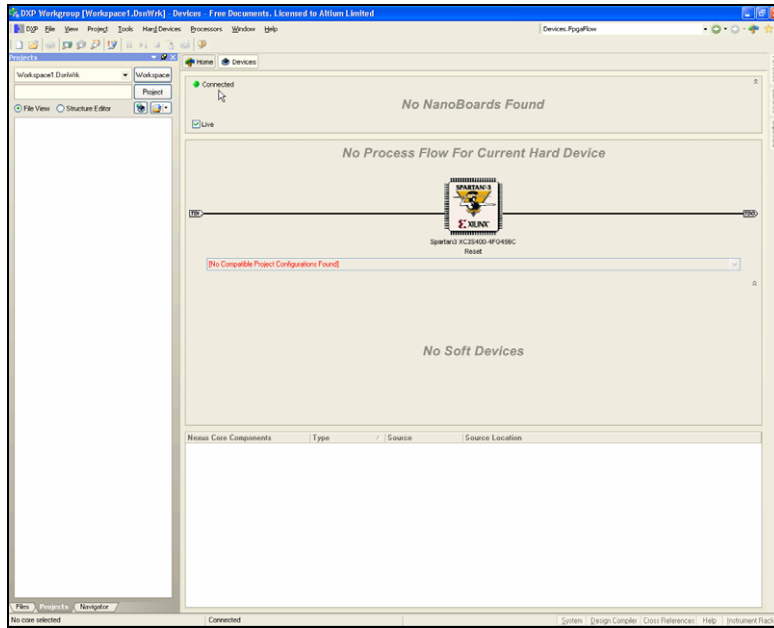
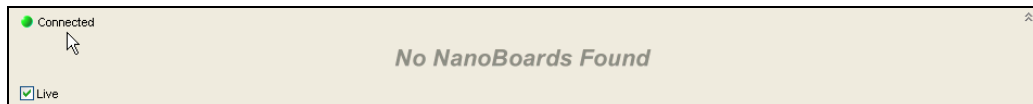


Figure 7. The Devices View window. Note: Xilinx Spartan-3 device shown. Image will be different depending on your target FPGA device

4. Ensure that the **Live** checkbox is enabled and that the **Connected** indicator is green. This indicates that the system is connected and communicating with the LiveDesign Evaluation Board.



5. If the Device does not show the LiveDesign Evaluation Board status as connected, or no FPGA icon is visible, refer to the *Troubleshooting connection problems* section later in this manual. The 'No NanoBoards Found' message will be shown, but is not relevant in the use of the LiveDesign Evaluation Board.

Downloading a test project to the LiveDesign Evaluation Board

To ensure that your design system and LiveDesign Evaluation Board are correctly installed and functioning, follow the steps below to compile and synthesize an example project and download it into the LiveDesign Evaluation Board. For this test, we will use the FPGA_LedChaser_EvalBoard.PRJFPG example found in the \Program Files\Altium2004\Examples\LiveDesign Evaluation Board\FPGA Hardware\LED Chaser - Hardware directory.

1. From the menus, select **File » Open**.
2. Navigate to the \Program Files\Altium2004\Examples\LiveDesign Evaluation Board\FPGA Hardware\LED Chaser - Hardware directory.
3. In this directory, open the file FPGA_LedChaser_EvalBoard.PRJFPG. When the project has loaded, the **Projects** panel on the left side of the workspace will display the files in this project.

If the **Devices** view is not active, select **View » Devices** from the menus to display it. The project open will automatically be assigned to the FPGA device on the active LiveDesign Evaluation Board. The figure below shows this for the Xilinx Spartan-3 device.

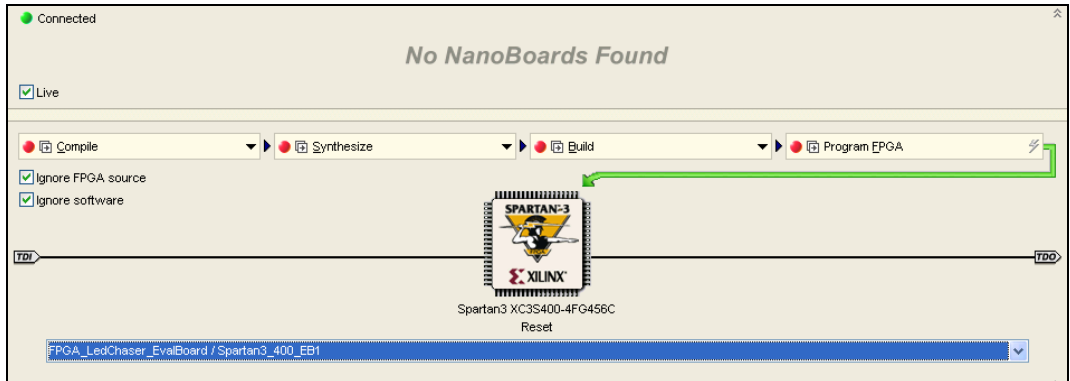
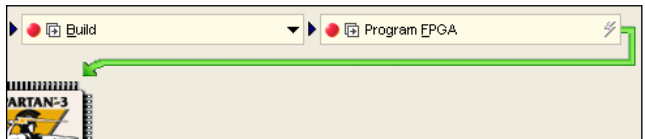


Figure 8. The Devices View window showing the Xilinx Spartan-3

4. To process the project and download it to the LiveDesign Evaluation Board, click the **Program FPGA** button in the **Devices** view.



The system will automatically compile the source project files, synthesize the design, call the vendor place and route tools to process the design for the target FPGA, and then download the design to the LiveDesign Evaluation Board. This can take several minutes depending on the speed of your computer.

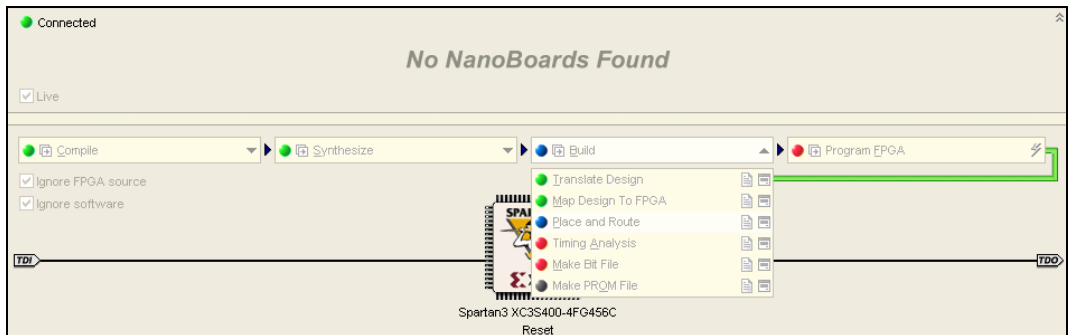


Figure 9. The Devices View window showing the compilation progress

Please note: If the system fails during the Build processes, it is shown by a purple status indicator. This can be because the FPGA vendor tools are not correctly installed or have not been properly activated. Please refer to the information supplied with the FPGA vendor tools for details on installing and activating these tools. For more details, visit www.altium.com/dxpcentral.

Once the design has been downloaded all of the process indicators will be green and the *Results Summary* dialog will be shown. This indicates that the project has been successfully processed and downloaded to the LiveDesign Evaluation Board. Close the *Results Summary* dialog.

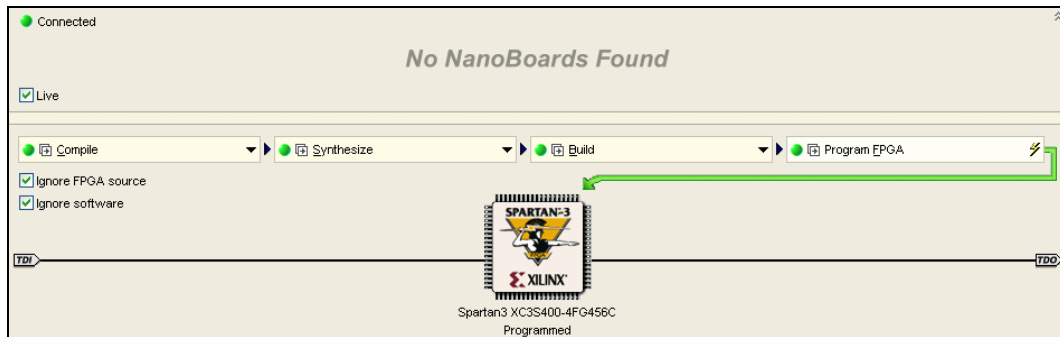


Figure 10. The Devices View window showing a successful compilation and download

Congratulations! You have just reconfigured your LiveDesign Evaluation Board to operate as a light chaser. If you look at the board you should see that the LED array above the 8 way DIP switch displays a moving pattern.

Please note that the **Devices** view now shows icons representing some virtual instruments (IO modules) running on the LiveDesign Evaluation Board.

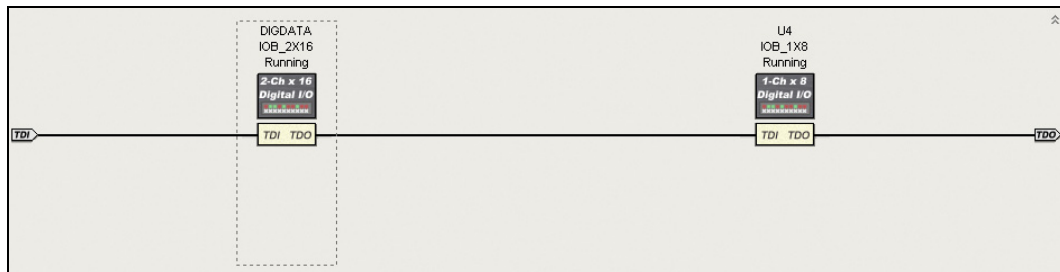


Figure 11. The Devices View window showing virtual instruments

In this project, the IO modules are used to control the operation of the LED chase sequence. The icons in the **Devices** view shows the system is communicating with these instruments running in the FPGA, allowing you to interact and control the instruments for development and debugging purposes. Explore the schematics in the `FPGA_LedChaser_EvalBoard` project for more information on the connection and operation of the virtual IO modules. Double-click on an IO module icon in the **Devices** view to access the front panel for that device.

Troubleshooting connection problems

If the **Devices** view shows that the system cannot connect to the LiveDesign Evaluation Board or cannot detect the presence of an FPGA on the LiveDesign Evaluation Board after completing the setup and installation procedures, go through the following steps:

1. Ensure that the LiveDesign Evaluation Board is powered and that the power LED next to the power supply socket is illuminated.
2. Ensure that the LiveDesign Evaluation Board to PC cable is correctly plugged in to both the PC and the LiveDesign Evaluation Board.
3. With the **Devices** view active (**View » Devices**), ensure that the **Live** checkbox is checked.

If the system still cannot establish a connection with the LiveDesign Evaluation Board and FPGA after completing all the above steps, then please contact your nearest Altium Sales & Support Center or Reseller.

Please note: The system requires the presence of a working, standard parallel port on your computer. The parallel port implementations on some computers do not strictly adhere to the standard, which may cause communications with the LiveDesign Evaluation Board to fail. If possible, reinstall the system on a different computer to determine if this is the problem.

Where to go to from here

Once you have completed the steps outlined in this guide, your system is installed and ready for use. To help become familiar with your design system and its features, we recommend you refer to the *LiveDesign Evaluation Kit Quickstart Guide* for additional examples and information.

Features & Peripherals

This chapter describes the LiveDesign Evaluation Board, its major components and how they interact. It also provides information on the LiveDesign Evaluation Board's various interfaces in detail. LiveDesign Evaluation Board schematics and PCB files are provided in the \Program Files\Altium2004\Examples\LiveDesign Evaluation Board\Reference Designs folder, and should be referred to as the final reference.

Specific examples have been included in the \Program Files\Altium2004\Examples\LiveDesign Evaluation Board\ folder to demonstrate the use of these features and peripherals. For more information, support resources and additional examples, refer to www.altium.com/dxpcentral.

The LiveDesign Evaluation Board was designed using Altium's Schematic and PCB Editors as a six layer printed circuit board. The internal routing capacity of the FPGA device used in the LiveDesign Evaluation Board has allowed PCB tracks to be optimally placed to minimize vias. Power and ground distribution is facilitated using a star topology. All unused copper areas have been flood filled with ground plane.

The PCB provides a good example of techniques required for using low cost medium speed FPGA devices with BGA footprints.

LiveDesign Evaluation Board outline and features

Figure 12 shown below presents an overview of the layout of the LiveDesign Evaluation Board, its various features and peripherals.

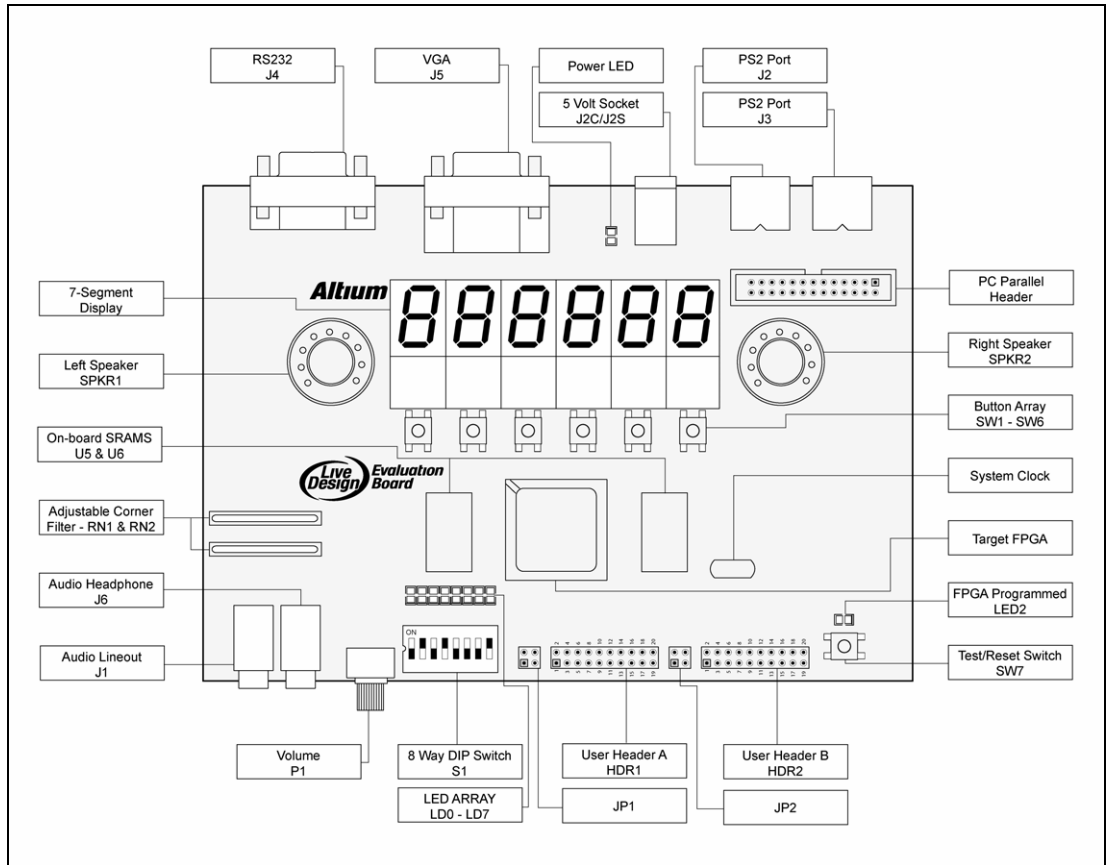


Figure 12. Physical layout of the LiveDesign Evaluation Board

Power Supply

The LiveDesign Evaluation Board is powered by a 5 volt regulated supply (included). Typical current requirements for the LiveDesign Evaluation Board, without any current supplied to expansion devices, is 100 to 500 mA. If the total power consumption of a given LiveDesign Evaluation Board configuration with connected expansion is greater than the standard 5 volt supply unit, then a higher current capacity power supply may be required. Such a power source must provide a regulated 5 volt DC supply.

The LiveDesign Evaluation Board has on-board regulators that provide various voltages depending upon the target FPGA. For example: +3.3 volts, 1.2 volts and 2.5 volts for the Spartan-3 and 3.3 volts and 1.5 volts for the Cyclone. Both the 3.3 volt and 5 volt supply buses can be selected to power various expansion devices that can be connected to the LiveDesign Evaluation Board.

The Peripherals

The LiveDesign Evaluation Board has a variety of resources individually wired to target FPGA IO pins. These allow a wide variety of embedded examples to be executed on the LiveDesign Evaluation Board, in addition to providing a base for developing new applications. Schematic library components are provided to allow the resources to be easily incorporated in designs. These are available in the FPGA LiveDesign Evaluation Board Port-Plug-in integrated library. An image of each component is shown with the following descriptions.

The library components automatically establish connectivity between the resource and FPGA IO pins, allowing the same design to be built for different FPGA devices from different manufacturers. The Configuration Manager enables a single project to be targeted at different FPGA devices. Library components can be placed into your FPGA design from the library `\Program Files\Altium2004\Library\Fpga\FPGA EvalBoard Port-Plug-in.IntLib`.

Specific examples have been included in the `\Program Files\Altium2004\Examples\LiveDesign Evaluation Board\` folder to demonstrate the use of these peripherals.

System Clock

The LiveDesign Evaluation Board has a clock generator that provides a fixed 50mHz clock. The clock signal is available in the FPGA, i.e. connected to a FPGA GCLK (global clock) pin.

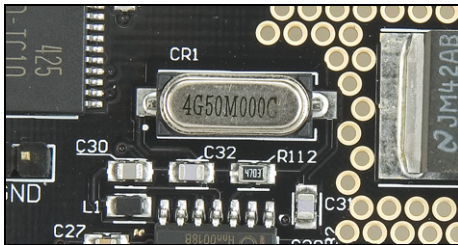
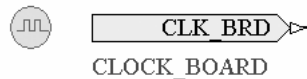


Figure 13. Fixed 50mHz clock



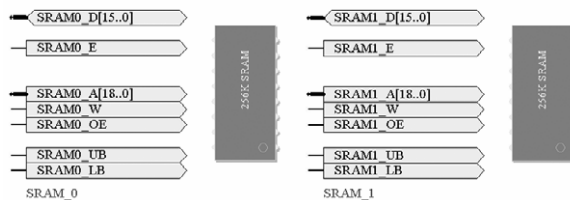
Static RAM

The LiveDesign Evaluation Board provides two 256k x 16 static RAM devices (SRAM0-U5 and SRAM1-U6), directly connected to I/O pins on the target FPGA. The SRAM devices are wired individually to FPGA I/O pins, so the SRAM may be configured in many ways by the FPGA IP.

The memory resource can be application-configured as a single 256k x 32 space, two 256k x 16 spaces, or a single 512k x 8 space. The 256k x 16 SRAM devices have an access time of 10 nS.



Figure 14. On-board SRAMS, U5 & U6



USER HEADER A and B

A total of 36 FPGA I/O signals are terminated on 20 pin headers USER HEADER A (HDR1) and USER HEADER B (HDR2), 18 signals per header. These headers also provide ground and either 3.3 volt or 5 volt power supplies, selectable using 4 pin supply select headers JP1 and JP2 respectively.

USER HEADER A and USER HEADER B are provided to allow user-defined hardware to be interfaced to the FPGA. The user header I/O pins can be configured as either input or output.

A range of devices with compatible 20 pin IDC header interfaces are available from various third party development board suppliers. For more information refer to www.altium.com/dxpcentral.

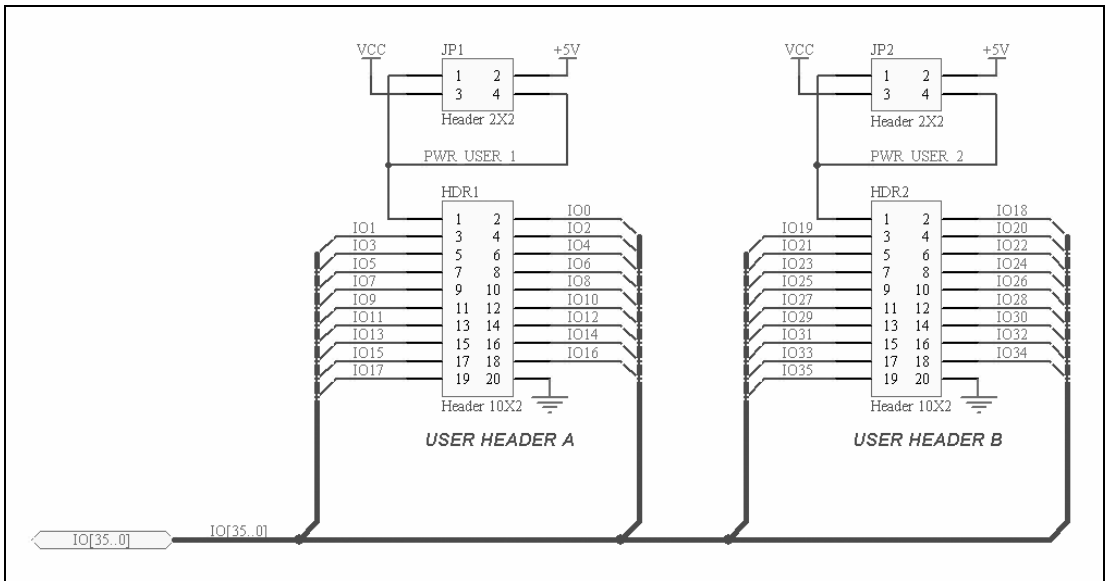


Figure 15. User I/O Pin Connections

RS232 Serial Port

J4 (DB9F) provides a DTE RS232 port, with signals TXD, RXD, RTS and CTS. These signals are derived from the LiveDesign Evaluation Board FPGA. Each of TX, RX, RTS and CTS signal has a LED, allowing RS232 data to be observed. RS232 level translation is provided by a MAX3232 device. For more information about this device refer to the Maxim website www.maxim-ic.com.

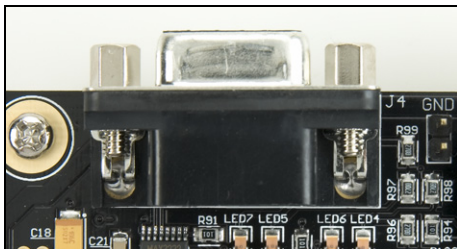
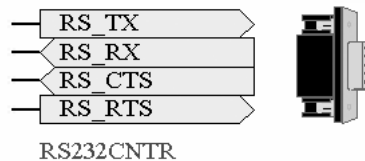


Figure 16. RS232 Port (J4)



Keyboard & Mouse Ports

J2 & J3 (MINIDIN) provide standard PS2 ports, nominally for use with a PC keyboard or mouse. These ports are directly connected to the FPGA I/O pins.

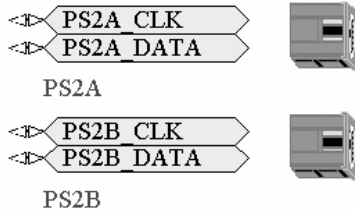
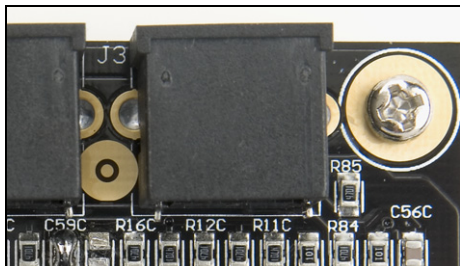


Figure 17. PS2 Ports

VGA Port

J5 (DB15) provides a VGA-compatible RGB video monitor port. The port is configured with three bits per color; a total of 9 bits per pixel or 512 colors. The port is directly connected to 9 FPGA I/O pins. Two additional FPGA I/O pins provide vertical and horizontal sync signals to the VGA connector.

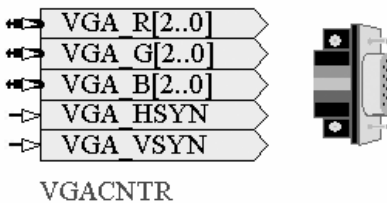
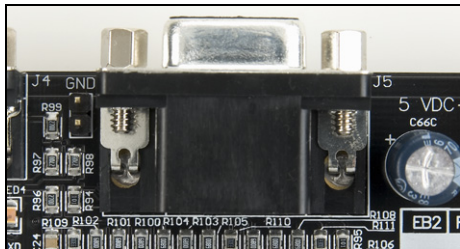
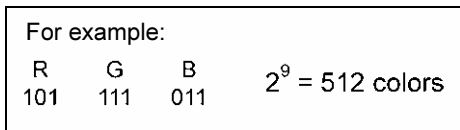


Figure 18. VGA Port (J5)

Audio System

The LiveDesign Evaluation Board contains a Delta-Sigma stereo audio output chain, providing 2.5mm stereo line out socket (J1), 2.5mm Headphone socket (J6) and two miniature speakers, SPKR1 and SPKR2. The headphone/on board speaker amplifier provides 100mW per channel. Volume control is provided for the headphones and speakers by potentiometer P1.

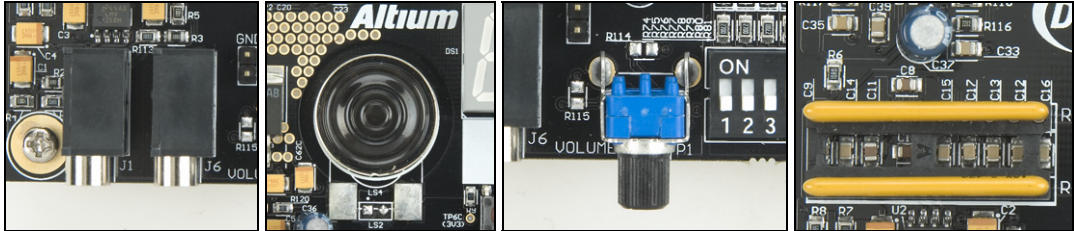
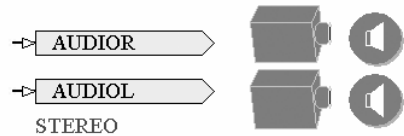


Figure 19. From left to right: Stereo line out and headphone sockets, speaker, volume control, inline resistor pack

The Delta Sigma sample rate is determined entirely in the FPGA depending on the audio application. Each audio channel has an output filter whose corner frequency can be adjusted by inserting a single inline resistor pack (RN1 and RN2) with five equal value resistors into the IC sockets available. The LiveDesign Evaluation Board is supplied with a corner frequency of 10kHz, but this can be adjusted over a wide range.



7-Segment LED Modules

The LiveDesign Evaluation Board comes with a six digit 7-segment display. Each segment and decimal point is driven by an individual FPGA output pin.

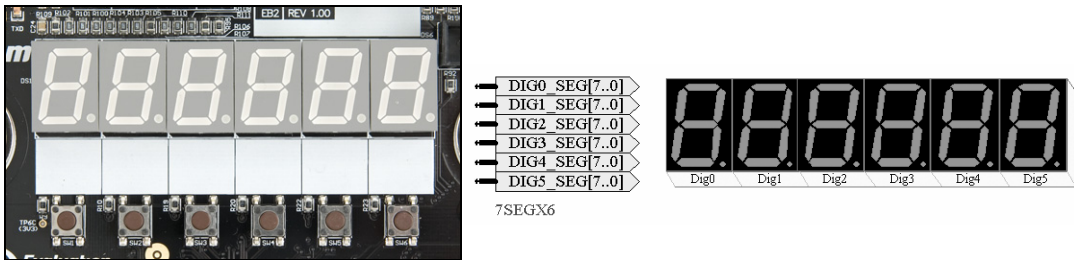


Figure 20. Six Digit 7-Segment Display

Keypad array

User input can be entered using the keypad array, which consists of six miniature pushbuttons (SW1 ... SW6) arranged in a 1 x 6 matrix. Each button is connected to an individual FPGA input pin. The button array has a region of white overlay above each button, allowing the function of each button in an application to be marked with a felt-tipped pen.

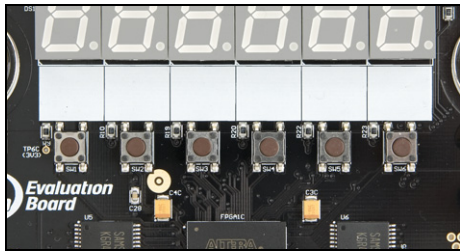
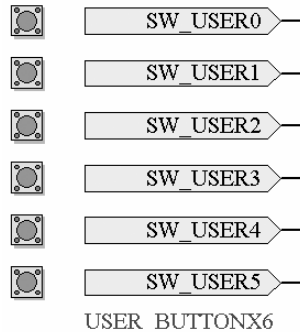


Figure 21. Six user input buttons



User DIP switch

The LiveDesign Evaluation Board provides an 8 way DIP switch S1 with each switch being connected to an individual FPGA I/O signal. The DIP switch is wired as an active low device, i.e. when the each switch is ON the signal produced is low.

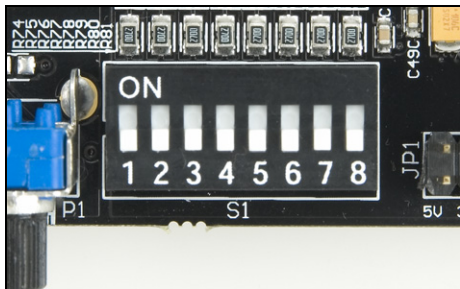


Figure 22. DIP Switch



LED Signal Outputs

The LiveDesign Evaluation Board has eight red LEDs (LD0 ... LD7), each driven by a separate FPGA signal. The LED signals are active high, i.e. a high level on the LED signal illuminates the LED.

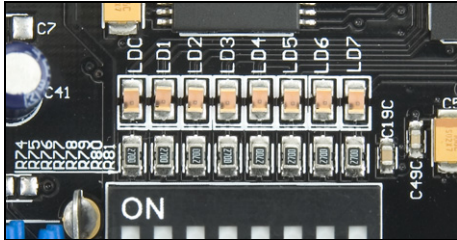
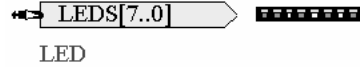


Figure 23. LED array



The LiveDesign Evaluation Board also has a LED marked LOADED above the TEST/RESET button that is illuminated whenever the target FPGA has been successfully configured. (LED2)

User-defined TEST / RESET Button

The LiveDesign Evaluation Board has a button (SW7) labeled TEST/RESET that is connected to a FPGA I/O signal. The button's function is entirely determined by the user application, i.e. it has no intrinsic function unless defined by the user application.

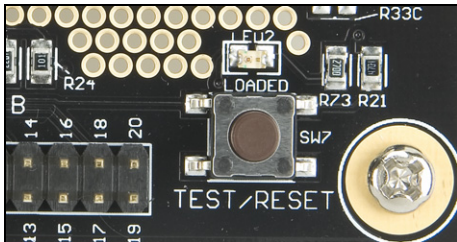


Figure 24. TEST/RESET Button



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