

Build 6.6.7903

PCB

- When drawing tracks in masked state, their net names remained distractingly bright. Net names are now dimmed consistently with their masked tracks.
- The polygon manager has been improved and now correctly remembers grid settings including column width and sort order.
- When a component is replaced in the design or a component footprint is modified due to an editing operation, its copper primitives are now properly assigned to the nets of their connected pads.
- View -> Selected Objects and View -> Filtered Objects commands are now available in the PCB Library Editor.
- Edit -> Slice Tracks command is now available in the PCB Library Editor.
- Component bodies on the bottom layer are now positioned correctly in the 3D viewer.
- 3D models originating from STEP files are now correctly orientated on the bottom of the PCB.
- A graphics system report has been added to the PCB display preferences reporting on the graphic capabilities of all displays.
- The drill drawing legend has been improved and now includes slot length details and has extended symbol capabilities.
- Now when using 'Make PCB Library' command the pads that contain slots/square holes will be correctly created in the PCB Library. The slots/square holes will no longer be reset to round holes.
- A message will be shown when loading/saving PCB libraries which contain duplicate footprint names.
- The DRC Markers will no longer be displayed in DirectX Mode when the DRCErrors layer is turned OFF.
- The file extension is now correctly set to .Rul when a simple filename is entered in the export rules dialog.
- An STG Exception will no longer appear when searching Altium Designer libraries for one or more PCB footprints.
- The NC Drill output report has been improved. No drill double hits will be generated in any of the NC Drill files.
- The IPC-D-356A netlist will now be correctly generated when Metric units are used for output.
- The print output of TrueType fonts has been corrected. True type text is no longer offset and is correctly replicated into embedded board arrays.
- Improve the speed of interactive net highlighting (Ctrl+Shift+Mouse Hover) in DirectX mode.

- Now the thermals and voids on Internal Planes will be drawn with the layer color when they are not in HideOtherLayers Single Layer Mode. This is the same rule applied when in GDI Mode.
- Top/Bottom SMT pads now display correctly all the time.
- The "AllLayers" Layers Set is now loaded correctly & includes all the layers in the board.
- Mirrored TrueType Text will now display correctly in DirectX mode.
- Support for the output of slots using the G85 command (drilled slots) has been added.
- DrillDrawing Legend generation will no longer crash the Gerber output when sorted data is generated & the Legend is outside of the board extents.
- Pads with a HoleSize = 1 unit will no longer be added to NC Drill output.
- Placing arcs in polygon pours will now display them as hollow arcs not as full circles.
- The DirectX test dialog shows a clear message of the status of the current display. Also the dialogs will have a Next button that moves to the next monitor & the dialog on the last found monitor will have a Finish button.
- Now the user will be able to get the X/Y offsets interactively before proceeding to move the selection. This way the objects can be moved very precisely relative to another object in board. The user can choose the offsets by clicking on 'Define X/Y Offsets interactively...' button and then choosing the start and end points of the selection move and the offsets will be automatically calculated from these two locations.
- Using 'Show all primitives in highlighted nets' will show all primitives in the highlighted net even if one of the Single Layer Modes is ON. This behavior is the same with that in GDI mode.
- When in DirectX mode the large selection bounding rectangle is shown when moving the selection. This now has the same behavior as experienced when in GDI mode.
- The Layer Stack Manager has been improved and now displays the total height of the stack-up.
- The pad dialog preview window tabs background is now drawn as transparent.
- Masked pads/vias are now drawn in DirectX mode the same way they are drawn in GDI mode. The hole color is dimmed as needed and the hole no longer disappears at certain zoom levels. Also when in single layer mode blind and buried vias will not display on layers that they shouldn't be visible.
- Blank trailing spaces on PCB footprint names are now correctly stripped and do not cause mismatches when compiling integrated libraries.
- Now when customizing the SetCurrentLayer command the TAB layer at the bottom of the PCB Window will also change accordingly.
- The via/pads that are inside a split plane will now update when the net of the split plane is changed.
- The Hyperlynx output will output the signal/plane layers in the correct stack-up order, in which the material properties will be taken from the database, instead of using defaults and the bulk resistance value being changed to $C=1.724e-8$.
- Browsing nets in the PCB Panel has been improved, and now correctly uses the current measurement units (imperial or metric).

- Speed has been improved and the drawing of cut-out regions is up to 7 times faster resulting in faster zooming and panning when the board contains many cut-outs.
- The height of Stroke Text objects will no longer be capped to 1 Inch. They will be unlimited like it used to be before TrueType fonts were added.
- Now the selected style value will be correctly saved and the bold style will no longer be automatically added, when changing the Font Style for any of the items that can be displayed in HeadUp.
- Blind/buried vias displays have been improved. Now they only display if at least one of the start/stop layers is visible.
- Single layer modes now function correctly when using DirectX with the Transparent Layers option on.
- Solder Mask Top/Bottom will no longer be shown when in Single Layer Mode when the current layer is a Plane Layer and the Solder Mask layers are turned ON.
- RebuildColors speed has been improved. This will speed-up panning in interactive processes, layer change and also net highlighting.
- No AV will appear when loading the daughter board NBP31.PcbDoc or any other PCBs that have dimension objects in them.
- Move Selection By X:Y offset now allows the user to enter the offsets manually as well as interactively.
- Endcaps will now be drawn on any selected arcs.
- The location of any text object in the HUD will now have the same location as shown in the status bar. The same applies to the location of the text object in the database.
- The component designator/comment rotation will now be loaded correctly.
- When in Single Layer Mode and current layer is a Plane Layer the pad shapes on signal layers will no longer be drawn.
- Pad/Via thermal reliefs will be displayed when you are in Draft Mode and the current layer is a Plane Layer.
- The Board Insight preview panel is now correctly updated when an object is hovered in a PCB document.
- The reporting of "Broken Net" design rule violations has been improved. Copper islands not connected to component pads will now be reported as 'Orphaned copper starting from: ' rather than generating empty 'Subnet:' strings.
- Net analyzer now correctly follows topology driven connections or manually created from-tos when 'Smart track ends' option is active.
- Situs performance has been improved for boards containing arcs in their outline.
- The differential pair rule retrieval has been improved.
- Pads are now correctly rotated when placing PCB components from the bottom side of the board.
- Identifiers containing parenthesis are now returned correctly from Situs to P-CAD.
- DRC report no longer report rules without violations in the body of error reports.
- Calculating characteristic impedance value from track width, when metric units are used, now produces a correct value.

- The memory management in DirectX mode has been improved resulting in significantly less consumption.
- Layers dialog has been improved. Changing mechanical layer status on large boards in DirectX mode, no longer causes delays.
- Selecting PCB filter examples no longer causes an access violation.
- Compatibility with third-party servers interfacing with the PCB module has been restored.
- An access violation occurring when editing the default pad with no PCB documents open has been resolved.
- An additional Pad shape designated 'Rounded Corners' has been added to PCB. This provides a true rounded rectangle shape with controllable corner radius. The existing 'Round' shape has been renamed to 'Rounded Ends' for clarity.
- The Pad Properties dialog has been improved. The preview window now defaults to multi-layer when editing multi-layer Pads.
- A new button has been added to the PCB panel allowing direct control over the navigation zoom level.
- The IPC Footprint Wizard now includes a generator for:
 - QFN (Quad Flat Pack No-Lead) components.
 - SOT143 footprints.
 - CQFP (Ceramic Quad Flat Packs).
 - PLCC (Plastic Leaded Chip Carrier) packages.
 - Generating SOT223 footprints.
 - Generating SOT23 5-Leads and 6-Leads footprints.
 - Chip Capacitor, Chip Resistor and Chip Inductor components.
 - Generating SOT23 3-Leads footprints.
 - SOT343 packages.
 - BQFP (Bumpered Quad Flat Pack) packages.
- All IPC Footprint Wizard generators now:
 - Allow the finish button to be pressed at any stage to generate the currently previewed footprint.
 - Show a preview of the footprint at every stage.
 - Include a footprint preview on most footprint generator pages reflecting the current footprint state, and a permanent finish button that can be pressed at any time within a generator to produce the final footprint as shown in the current preview.
- IPC Footprint wizard now has a SOIC/SOP J-Leads footprint generator.
- The PCB filter panel now functions correctly when docked to a window without any open documents.

Schematic

- The Database Table Name field can now be edited using the SCH List panel or the SCH Inspector.

- Pin swapping has been improved: an AV no longer occurs after pushing pin swaps back to the schematic and doing and then undoing. The swapped net labels are no longer flipped upside down.
- A new tool has been added to measure the distance between two points. In the Reports menu, select the Measure Distance tool, then choose two points to determine the distance.
- The schematic editor has been improved. Problems with the display of lines at minimum zoom-level have been fixed.
- The schematics library command 'Update Schematics' has been improved. Comments with empty strings or '*' as their texts will be automatically set to the library reference.
- The schematic library saving process has been improved and images are now saved correctly.
- The create sheet symbol from sheet command has been improved. Sheet entry sizes are now taken into account so that they do not overlap.
- The parametric hierarchy feature has been improved. Printing and SmartPDF now take this into account.
- The schematics file loader has been improved. Loading sheets with polygons of more than 50 vertices is now possible.
- The schematic filter panel has been improved. Hints now work correctly when the scope is set to open documents from the same project.
- The Schematic function has been improved. Setting the width of a port to zero, will no longer causes a crash.
- Schematics has been improved. Failed component placement from the library panel no longer causes the undo command to be disabled.
- Schematics has been improved. Part designators where the part IDs are greater than 26 are now displayed correctly (as AA, AB and so forth).
- Cut, Copy and Paste functions are now available through the right-click popup menu.
- Smart Paste has been improved. Smart Paste by location with expanded buses will now keep the original net order.

FPGA

- It's now possible to add SDC, GCF and PDC files to the project and have them used by the Actel® Place and Route flow.
- The system will now correctly detect Altera® Quartus 3.0 and 3.1.
- The flow stage now accurately shows the result of the Quartus synthesizer version 6.0 and onwards. Previously a successful run was being reported as a failure.
- The issue that was causing FPGA/CORE projects to compile slowly has been resolved. Compile times should be visibly faster on large projects.
- A possible combinatorial loop involving bad decodes for the WB_INTERCON component has been resolved.
- The issues with Actel® BGA devices with the port 'P' not being exported properly both in the PCB->FPGA Synchronizer as well as the vendor constraint files have now been resolved.

- Whenever an error occurs in the flow, the FPGA flow stage will now properly fail. Previously you could continue if the vendor process still generated the output file.
- Added recognition of all supported FPGA vendor constraints documents in the system. This will facilitate the easy use and addition of vendor constraint documents to a project.
- FPGA_CLOCK_FREQUENCY no longer requires a corresponding FPGA_CLOCK or FPGA_GLOBAL constraint to activate. So this parameter can be used when clocking is done manually by the user. However, this parameter can still only be used on valid clock signals.
- The issue experienced when incorrect HDL code was generated when connecting a port to a pin using reversed bus notation has been resolved.
- Configurable Memory Component has been improved to support more SDRAM memory layouts. Supported memory layouts are:
 - 1 Device x 32 bit
 - 1 Device x 16 bit
 - 1 Device x 8 bit
 - 2 Devices x 16 bit
 - 2 Devices x 8 bit

System-Level

- Support for SVN over SSH (Secure Shell) has been added.
- CVS now supports the ext protocol to allow the running of the communication over SSH (Secure Shell).
- Sorting by the Date Modified field in the Files section of Storage Manager, now sorts correctly.
- The default SVNDBLib Working Folder has been moved into the My Designs folder instead of the Temp folder.
- The SVN Checkout dialog has been simplified to make it easier to use.
- The PADS Importer has been improved so that additional bogus vias are no longer created.
- The variant output subsystem has been improved and:
 - BOM file name format will now take variant names into account. When no variant is selected, the file name format will remain the same, which is <Bill of Materials>-<Project Name>. If there is a variant selected, then the file name format will be <Bill of Materials>-<Project Name> (<Variant Name>).
 - When running the BOM dialog directly from schematics, a choice of which variant to use can now be made.
 - When printing variants on schematic sheets, a choice can be made on how to draw the components that are not fitted. You can select a red cross, gray mesh box, or user-specified text.
 - A detailed report that includes all the parameter variation values can now be generated.
- The P-CAD importer has been improved so that layer names and layer stacks are now imported.

- The variant subsystem has been improved.
 - Reports can now be configured to show just the differences between 2 or more variants.
 - Assembly print output jobs now allow the display of not fitted components to be configured.
 - Both grids in the dialog now support type-ahead search.
 - Double-clicking on a row in the component grid will automatically cross probe to the right component.
 - Selective batch replacement of parameter values from library can now be performed.

- The P-CAD importer has been improved so that patterns that are not linked to any component are now imported.
- The P-CAD exporter has been improved so that the '\' negation character is now properly exported.
- The OrCAD® exporter has been improved. The issue with pin name fonts being exported incorrectly has now been resolved.
- The library panel has been improved. Column widths for DB libraries are now remembered.
- The variants subsystem has been improved. Variant information is now preserved during re-annotation.
- The PCB Print Preview dialog has been improved. The crash experienced while zooming no longer occurs even if invalid values have been entered into the configuration options.
- The P-CAD importer has been improved so that imported polygon pad shapes now obey the pad rotation.
- The BOM report generator has been improved. When using older Excel versions the size of the columns can be limited. This is now taken into account when the report is exported as Excel files.
- The P-CAD importer has been improved. PCB files with NULL characters can now be imported.
- The BOM exporter has been improved. Numeric fields like quantity are now exported properly.
- The BOM exporter has been improved. PCB and schematic parameters can now be included together.
- The variant subsystem has been improved.
 - A special string can now be placed on schematic sheets indicating which variant is being printed.
 - SmartPDF now supports variants.
 - Schematic output jobs now support printing of physical documents including variant information.
- The P-CAD importer has been improved so that a clearer warning is now given on which types of P-CAD files can be imported.
- The PADS importer has been improved so that layers with no layer names are now correctly dealt with.

- The project parameter dialog has been improved and the dialog now recognizes newly edited parameter values.
- The variant dialog has been improved:
 - Multiple variant fittings can now be edited together.
 - A whole variant can now be copy and pasted.
 - The component and parameter variation grids can now be configured to show only the values that are different from the original.
 - An invert selection tool is now provided in the popup menu.
 - The order of the variants can now be changed.
 - The dialog now has a context sensitive mode, which will only show components that are selected on the schematic sheets.
- The schematic compiler has been improved. Tolerance issues experienced with metric sheets have been resolved.
- The BOM generator has been improved so that library references are now correctly exported.
- The BOM generator has been improved so that the fields 'Force Columns to Fit' and 'Include PCB Parameters' are now saved.
- Output jobs has been improved so that the document scope '[Project]' no longer causes a warning to pop up when the file is being loaded.
- The Multi-wire netlist generator has been improved so that it outputs bus net correctly.
- Snippets has been improved so that Names can now contain the '.' character.
- The PADS importer has been improved so that missing font styles in texts in ascii library files no longer cause the importer to hang.
- The OrCAD® DSN importer has been improved so that Polylines are now imported.
- The localization issue in the design rules dialog has been improved. Saving and loading of tree lists from the registry is now possible.
- When a project is created from a template containing external files (such as .Doc files), these files are no longer automatically opened separately when the project is created.
- Toolbars layouts are now correctly restored after Altium Designer restarts.

Embedded

- If closed properly the watches view doesn't pop up after restarting the system.
- In the Watches View, watched structures will now remain expanded while debugging and stepping through the code.
- Deleted expressions in Watches view no longer reappear after restarting Altium Designer.
- Evaluate view stays in focus after evaluating an expression, which allows you to evaluate multiple expressions without using your mouse to refocus the view.
- C-lib and DSF functions/symbols are now highlighted in code editor and can be navigated as well as functions/symbols in project.
- Registers panel now remembers visibility of columns set by user.

- Command 'open document under cursor' in .c or .h files now searches for files in all include paths of current project and in the dsf folder.

Signal Integrity and Simulation

- Component parameters are now given priority over Model parameters when entering parameter values into the XSpice netlist. This removes confusion when there are two parameters of the same name in existence at different levels.

CAM Editor

- ODB++ import in CAMtastic will work correctly even if the decimal separator is comma and the design contains solid polygons.
- Circular board outlines or outlines that only contain arcs can now be routed.
- The polygons and polygon voids will be eliminated from the Solder Bridging check. Invalid violations will no longer appear.
- Now the slotted holes thermals (oval thermals) will be exported to ODB++ even if they are not rotated.
- Full circles will no longer be created from small arcs when an embedded board array is exported to Gerber.
- DXF files exported from CAMtastic containing FAB drawing will load correctly in AutoCAD (2004 or later).