

## Ensuring the integrity of your signals

---

*One of the critical factors in creating boards that are correct by design prior to prototyping or PCB production is maintaining the integrity of high speed signals. Altium Designer's unified Signal Integrity Analyzer provides a powerful set of features to help you ensure that your design will work as expected in the real world. Here we show you how.*

In the world of high-speed digital design, a similar situation is played out, with noisy signals affecting their quieter neighbors to the extent that they can't deliver their 'messages' accurately. As higher speed devices become more common, the need for distributed circuit analysis at the board design stage becomes crucial. Where signals are produced with edge rates under a nanosecond, careful analysis of board impedances is necessary to ensure proper termination of signal lines, minimizing reflections on those lines and ensuring electromagnetic interference (EMI) falls within often regulated guidelines. Ultimately, you need to ensure the integrity of the signals across the board or, put another way, achieve good signal integrity.

### Ensuring the integrity of high speed signals

High-speed devices are making their presence felt in an ever-increasing number of digital designs these days. With such devices comes fast signal edge rates. For the designer, the concern becomes one of ensuring the integrity of the signals on the board. Fast rise times coupled with lengthy routing can result in signal reflections. Reflections apparent on a particular transmission line can not only impair the true signal data traversing that line, they can also induce 'noise' on neighboring transmission lines – the dreaded electromagnetic interference (EMI).

To monitor and control signal reflections and cross-signal interference (crosstalk), you need access to a tool that will allow you to analyze in detail the extent of reflections and crosstalk associated to any of the signals in your design. Altium Designer provides just the ticket!

### Performing signal integrity analysis in Altium Designer

Altium Designer provides a fully integrated Signal Integrity Analyzer that can be accessed during both the design capture (Schematic-only) and board layout phases of a design. Sophisticated transmission line calculations and I/O buffer macro-model information is used as input for the analysis simulations. Incorporating fast reflection and crosstalk simulators, the analyzer produces accurate simulations using industry-proven algorithms.

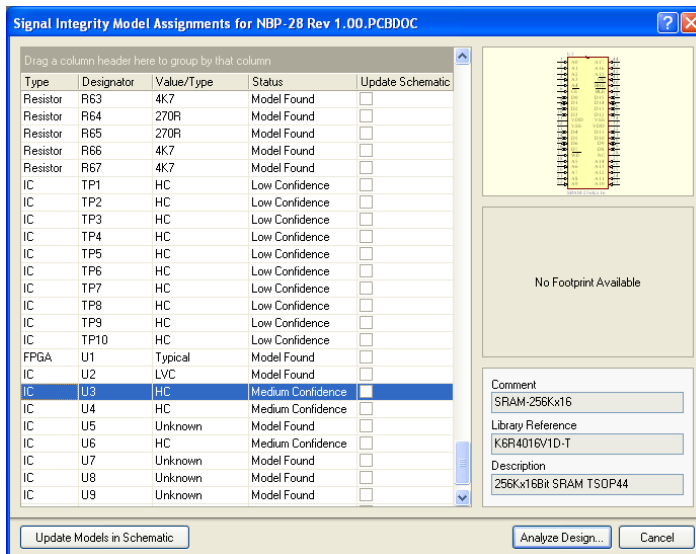
**Note:** Whether running a schematic-only analysis or analysis from a routed board, the schematic or PCB document must belong to a project. If a PCB is present, analysis will always be based on the PCB document.

## Important pre-analysis preparation

Eager to start analyzing? We're almost there, just a few things that need to be set up, without which the analysis results will be inaccurate and therefore pretty meaningless.

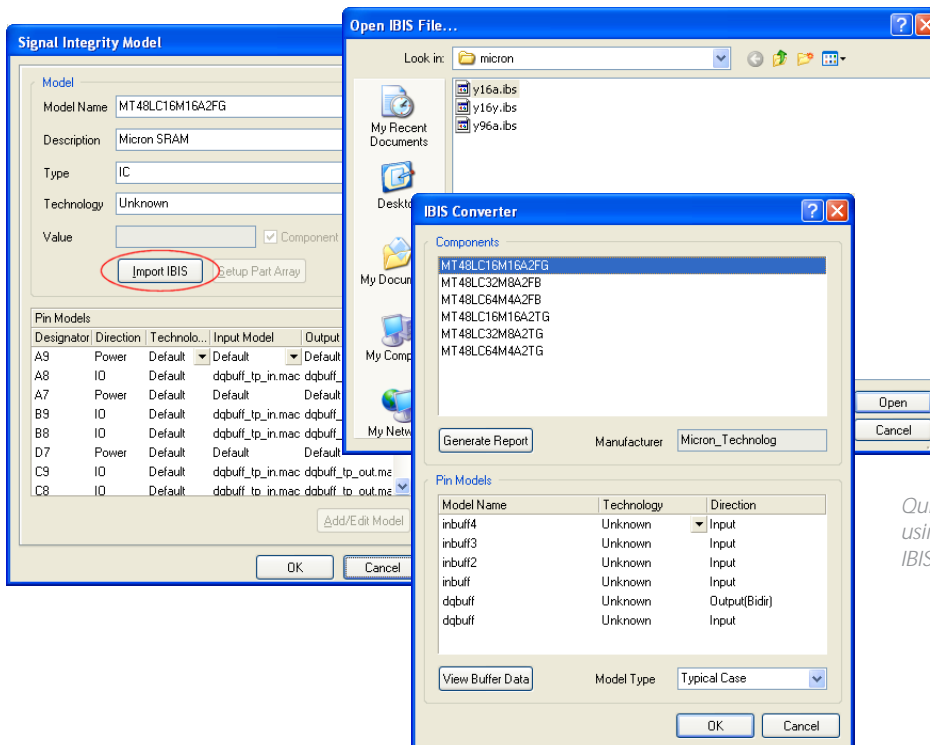
**If patience is a virtue, proper preparation is a Godsend.**

1. Not all nets can be analyzed for signal integrity characteristics. In order to analyze successfully for all characteristics, a net must contain at least one IC with an output pin. Resistors, capacitors and inductors will not simulate for example, because of their lack of output pin to provide a driving source. When bi-directional nets are analyzed, both directions are simulated and the worst case result is displayed.



2. The signal integrity model type for each component in the design must be correct. This can be defined using the Signal Integrity Model Assignments dialog. If models are not defined for all components, you will be given the opportunity to access this dialog when launching the Analyzer. Alternatively, you can adjust the models directly from the schematic by editing the respective model link for each component – double-click on the model link to access the Signal Integrity Model dialog.

*Reduce guesswork by ensuring model types are defined correctly for each component in your design.*



*Quickly import pin models using manufacturer-supplied IBIS model files.*

- Design rules must be setup for each of the supply nets in the design. There should always be at least two rules – one for power nets and one for ground nets. From a PCB, simply define the rules in the PCB Rules and Constraints Editor dialog (Design » Rules). Where no PCB exists for the design project, you can specify these rules by adding the appropriate PCB Layout directive to each required net. Alternatively, you can specify these constraints as part of the SI Setup Options dialog – more on that later.
- When performing analysis from the routed board, you must ensure that the layer stack for the PCB is defined correctly. The Signal Integrity Analyzer requires continuous power planes. Split planes are not supported, so the net that is assigned to the plane is used. If they are not present, they are assumed, so it is far better to add them and set them up appropriately. The thickness for all layers, cores and prepreg must also be set correctly for the board. These properties, as well as dielectric values, can be defined in the Layer Stack Manager dialog (Design » Layer Stack Manager). When running pre-layout analysis, a default two-layer board with two internal planes is used for calculative purposes. If you need more control, simply add a blank PCB document to your project and define the layer stack as required.
- Although not required, you could also define a Signal Stimulus design rule – either as a standard rule on the PCB side or a document-level parameter on the schematic side. The stimulus is the signal injected at each output (driving) pin on a net being analyzed. This would be done if you wanted to override the default stimulus setting.

## Running the signal integrity analyzer

The Signal Integrity Analyzer is accessed from the schematic or PCB using the Tools » Signal Integrity menu command. If you haven't defined models for all components, the Analyzer will attempt to guess which ones to use. If any models remain undefined, a warning dialog will appear. Depending on the signals you are interested in analyzing, you can either continue with the analysis or stop to tidy up model definitions – simply click Continue or Model Assignments as appropriate.

For more detail on setting up and running a Signal Integrity analysis, refer to the tutorial [TU0113 Performing Signal Integrity Analyses](#).

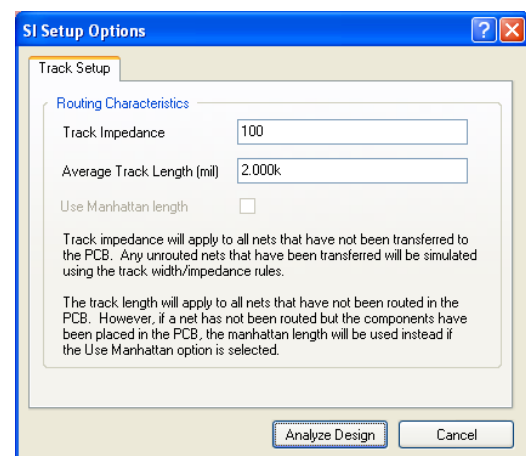
## Setting default routing characteristics

The first time you run the Signal Integrity Analyzer for a project, whether a PCB document is present or not, the SI Setup Options dialog will appear. Use this dialog to define default values for Track Impedance and Average Track Length.

When no PCB is present (pre-layout analysis) these values will be used by the Analyzer to gain an accurate picture of the likely **signal integrity** performance of the design. The value for the length should therefore realistically reflect the dimensions of the intended board. For pre-layout analysis, the SI Setup Options dialog can be accessed at any time from within the Signal Integrity panel. The dialog will also include tabs for defining Supply Net and Stimulus rules, if not already defined on the schematic.

When a PCB is present (post-layout analysis) the Track Impedance will only be used for nets not taken across to the PCB. Any unrouted nets already transferred will use the applicable width/impedance rules. The Track Length will apply to unrouted nets. However, if you have placed components, you can opt to use the Manhattan length for these nets.

Once options/models have been defined as required, the analysis will proceed and the **Signal Integrity** panel will appear – and that's where the fun really begins...



*Define default routing characteristics to be used where no actual routing is present*

## Initial screening analysis

The Signal Integrity panel lists all nets in the design (excluding power nets). The Analyzer performs an initial fast analysis on all nets in the design, called a screening analysis, with the results being listed down the left side of the panel.

### These results can include:

- Net data (e.g. total trace length and whether the net is routed)
  - Impedance data
  - Voltage data (e.g. overshoot and undershoot)
  - Timing data (e.g. flight time).
- Use the right-click Show/Hide Columns sub-menu to determine which data is displayed in the panel. By default, only undershoot and overshoot results will be displayed. These are the best characteristics to use in determining which nets may be the most problematic.

Net	Status	Falling Edge Overshoot	Falling Edge Undershoot	Rising Edge Overshoot	Rising Edge Undershoot
D2	Failed	3.410	2.696	3.385	2.698
D1	Failed	3.410	2.696	3.385	2.698
D0	Failed	3.410	2.696	3.385	2.698
D3	Failed	3.410	2.696	3.385	2.698
D6	Failed	3.410	2.696	3.385	2.698
D15	Failed	3.410	2.696	3.385	2.698
D7	Failed	3.410	2.696	3.385	2.698
D10	Failed	3.410	2.696	3.385	2.698
D8	Failed	3.410	2.696	3.385	2.698
D13	Failed	3.410	2.696	3.385	2.698
D5	Failed	3.410	2.696	3.385	2.698
D4	Failed	3.410	2.696	3.385	2.698
D12	Failed	3.410	2.696	3.385	2.698
D9	Failed	3.410	2.696	3.385	2.698
D11	Failed	3.410	2.696	3.385	2.698
D14	Failed	3.410	2.696	3.385	2.698
D20	Failed	2.649	2.108	2.670	2.100
D18	Failed	2.649	2.108	2.670	2.100
D27	Failed	2.649	2.108	2.670	2.100
D21	Failed	2.649	2.108	2.670	2.100
D26	Failed	2.649	2.108	2.670	2.100
D17	Failed	2.649	2.108	2.670	2.100
D25	Failed	2.649	2.108	2.670	2.100
D24	Failed	2.649	2.108	2.670	2.100
D29	Failed	2.649	2.108	2.670	2.100
D31	Failed	2.649	2.108	2.670	2.100
D16	Failed	2.649	2.108	2.670	2.100

Interrogate initial screening analysis results to identify problem nets in the design.

- Screening is a coarse-level analysis, used to quickly identify potential problem nets, which can then be analyzed in more detail. To further analyze one or more nets, they need to be taken over to the right hand side of the panel, where a reflection or cross talk analysis can then be performed. Move a net across either by double-clicking on it or using the available single arrow button.

## Detailed reflection analysis

As part of its arsenal of analysis tools, the Signal Integrity Analyzer incorporates a Reflection simulator. The simulator calculates voltages at nodes of a net using routing and layer information – from the PCB or from the default routing characteristics specified – and associated driver and receiver I/O buffer models. A 2D-field solver automatically calculates the electrical characterization of the transmission lines. Modeling assumes that DC path losses are small

enough to be ignored.

One or more nets can be simulated. Bear in mind that the analysis time will increase considerably when analyzing a higher number of nets.

To run the analysis, click on the Reflections button

## Detailed crosstalk analysis

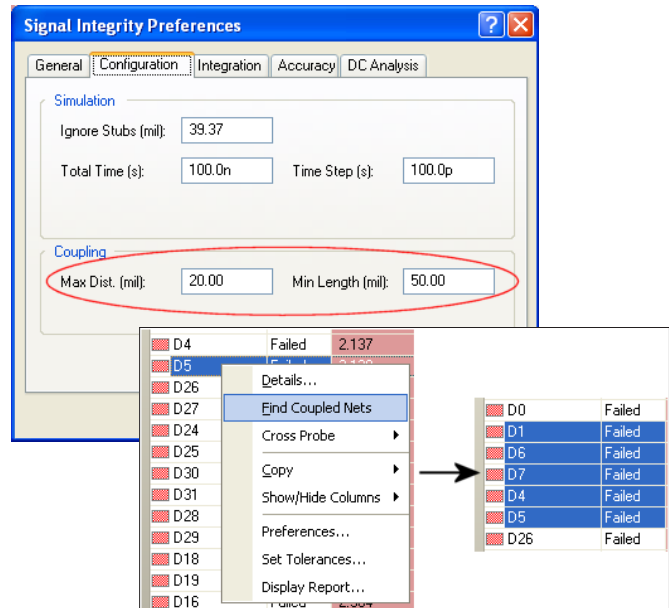
The Signal Integrity Analyzer includes a dedicated crosstalk simulator, allowing you to analyze the interference between coupled nets. Note that crosstalk analysis can only be performed from the PCB as routed nets are required for this type of analysis.

Two or three nets would normally be considered at any one time when performing a crosstalk analysis – usually a net and its two immediate neighbors.

The Signal Integrity panel includes a feature that enables you to quickly identify which nets are considered to be coupled, to the selected net(s) you choose. This feature – Find Coupled Nets – is ideal for working out which nets may be susceptible to crosstalk. It essentially analyzes the PCB and identifies traces that run parallel to each other according to defined coupling options.

The simulator allows you to specify a victim or aggressor net. Specify a net to be the victim if you want to analyze the interference on this net, generated from its neighbors. Specify a net to be an aggressor if you want to analyze the interference imparted from this net to all other coupled nets.

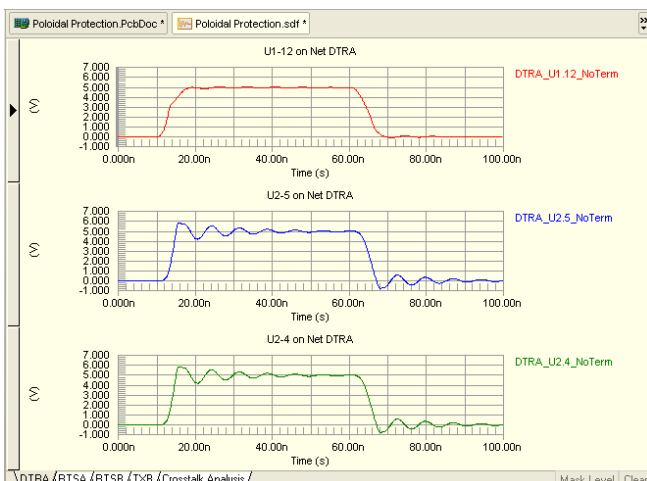
To run the analysis, click on the crosstalk button.



*Quickly identify nets that are coupled to a particular problem net of interest.*

## Displaying analysis results

As an analysis proceeds, a simulation data file (\*.sdf) will be generated and opened to display the analysis results in the Simulation Data Editor's waveform display window.



In terms of reflection analysis, the SDF file will include a chart for each net analyzed, with a waveform (plot) for each pin in the net.

The display of data for the crosstalk analysis chart is essentially the same as that for a reflection analysis chart. The only difference being that there is only a single chart for this analysis type, containing a plot for each pin in each net considered in the analysis.

For more information on working with analysis waveforms, refer to the application note [AP0106 Working with the Sim Data Editor](#).

*Analysis results are presented in the Simulation Data Editor.*

## Balancing transmission line impedances

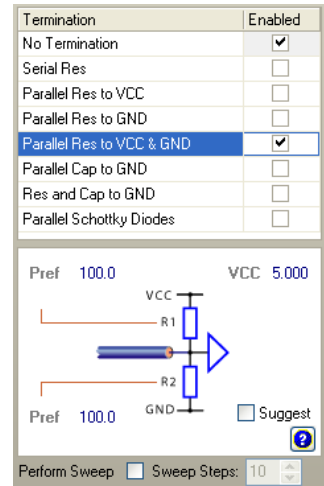
The key to achieving a successful design, in terms of signal integrity, is to get good signal quality at the load. Ideally, this means zero reflections (no ringing). Zero reflections may not always be possible in the real world, but the level of ringing can be reduced to an acceptable level for the design, through the use of a termination.

The Signal Integrity Analyzer incorporates a Termination Advisor, accessed from within the Signal Integrity panel, which enables you to insert 'virtual terminations' into a net at a location you define. In this way, you are free to test various termination strategies, without making physical changes to your board.

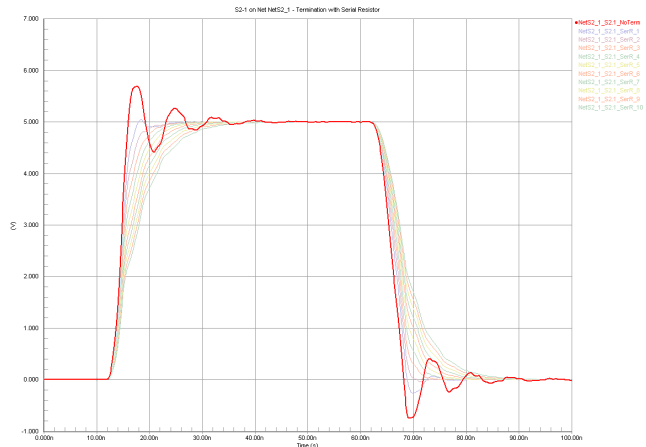
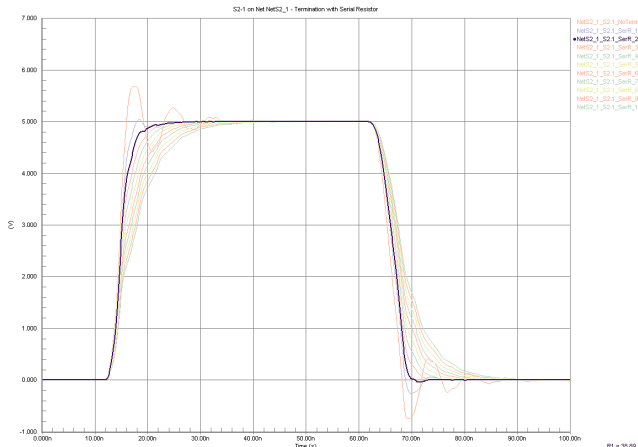
Eight different termination types are available, including the default No Termination. Multiple termination types can be enabled when performing reflection and crosstalk analyses – a separate set of waveforms will be produced for each. This allows you to determine the best termination to add to the design to achieve optimal signal quality on transmission lines and therefore reduce reflections to an acceptable level.

You can also run analyses using a swept range of termination component values. To do this, enable the Perform Sweep option and specify the number of Sweep Steps. If Sweep Steps is 2 for example, then the first pass of the analysis will use the minimum value specified for the component(s) and the second pass the maximum value.

Once the desired termination strategy has been found, you can place that termination directly on the schematic. You have full control over which library components to use, whether to place on all applicable pins or just the selected pin, and the exact values for the components. You simply have to wire the additional termination circuitry to the relevant pin.



*Try out a range of virtual terminations and values to match impedances and reduce reflections and crosstalk.*



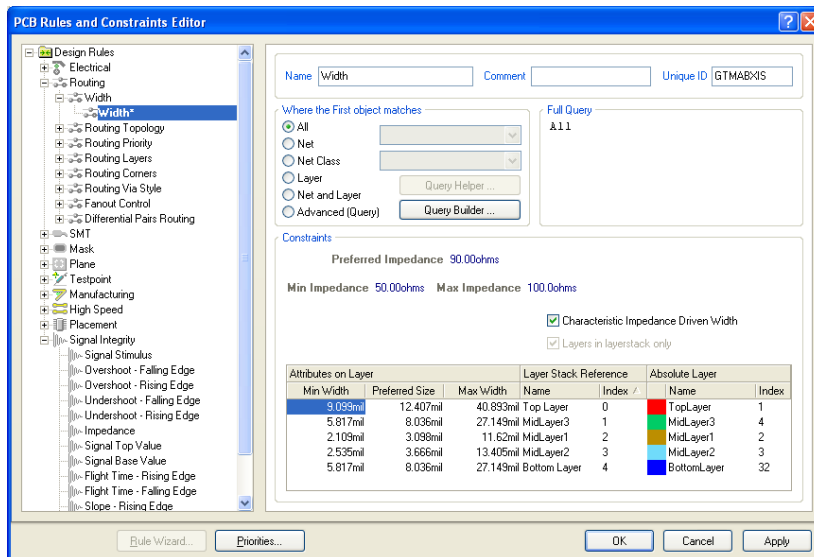
*If you have run the analysis prior to laying out the board, things are made even simpler, as you will not have to resynchronize with an existing – and possibly densely routed – PCB.*

## Impedance-controlled routing – now there's luxury

Reflections are caused by mismatched impedances. So far, we've discussed addressing this mismatch at the component-pin level, adding an appropriate termination to better match the impedance of the receiving pin to the impedance of the driving pin. Wouldn't it be neat if the actual transmission line – the routed trace on the board – could also be made to give the required impedance. No problem, Altium Designer's got you covered.

Altium Designer's PCB Editor lets you specify the impedance required and calculates the routing width required on each layer to achieve this. Simply enable the Characteristic Impedance Driven Width option when defining the Routing Width design rule in the PCB Rules and Constraints Editor dialog, then enter the required min/preferred/max impedances. These will automatically be translated into widths for each signal layer, to suit the physical layer properties you have defined.

Note: Impedances are calculated using formulae defined in the Impedance Formula Editor dialog, accessed through the Layer Stack Manager dialog (Design » Layer Stack Manager).

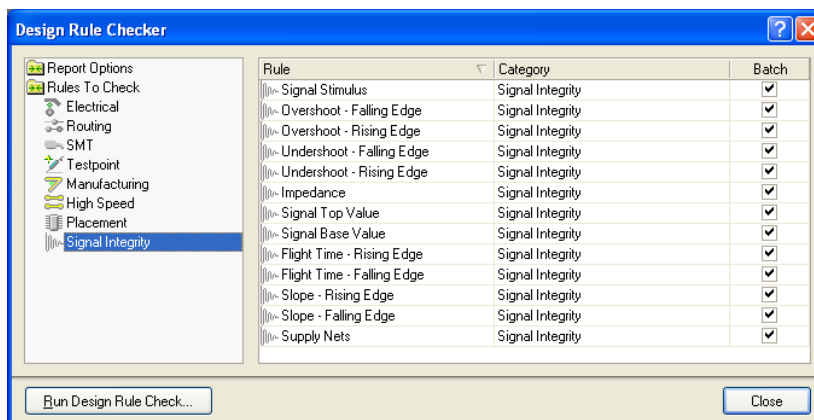


Specify your minimum, preferred and maximum impedance requirements and the routing widths for each signal layer will be calculated for you.

For further information, refer to the application note [AP0107 Impedance-Controlled Routing](#).

## Integrating signal integrity into standard board design flow

Prior to generation of manufacturing output, you will undoubtedly (and religiously) run a final design rule check (DRC). As part of its Batch DRC, Altium Designer's PCB Editor enables you to define various signal integrity-based rules. You can set thresholds for parameters such as undershoot and overshoot, edge slope, signal levels and impedance values. If a problem net is found during the checking process, you can run a more detailed reflection or crosstalk analysis.



In this way, setting up acceptable signal integrity parameters becomes part of the normal board definition process, in much the same way as you routinely define object clearances and routing widths. Identifying signal integrity problems caused by the physical layout then becomes a natural part of performing a complete DRC of the finished board.

Consider the signal integrity design rules as a complementary check, not as the sole means of analyzing your design.

Specify signal integrity rule checking as part of your routine DRC strategy.

## Signal Integrity in action – showcase examples

A number of example projects are included with Altium Designer that demonstrates the capabilities of its Signal Integrity Analyzer.

**These examples can all be found in the \Examples\Signal Integrity folder of the installation:**

- Differential Pair – this example (DifferentialPair.PrjPcb) illustrates reflection analysis of a simple differential pair transmission line.
- NBP-28 – this example (NBP-28.PrjPcb) illustrates how signal integrity analysis can be used to find optimum drive settings for specific pins of an FPGA device. This is almost a reverse approach to signal integrity analysis. Rather than having a design with signal integrity issues and fixing it through analysis of the problem nets, this example throws down the gauntlet “ how hard can specific signals in this design be driven before signal integrity and EMI issues become a problem?”
- Simple FPGA – this example (SimpleFPGA\_SI\_Demo.PrjPcb) illustrates the use of signal integrity analysis with a very simple FPGA design. In particular, it shows use of various termination types to reduce reflections on the transmission lines connected to different banks of the physical FPGA device (a Spartan IIE).
- Spirit Level – this example is really a collection of staged projects that follow the use of signal integrity analysis along the life of a real-world design – yes, the spirit level physically exists and accurately determined that my office shelves are not level! Each project ‘stage’ takes you through discovery of signal integrity issues and their resolution, first during the design capture phase (SCH Issues.PrjPcb and SCH Issues Resolved.PrjPcb) and then on to the board layout phase (PCB Issues.PrjPcb and PCB Issues Resolved.PrjPcb).

## The bottom line

In its Signal Integrity Analyzer, Altium Designer offers you the tool to ensure both signal integrity and EMI conditions are achieved within specification. With its support for pre-layout analysis, problems can be identified and remedied early in the design process. Prior to prototyping, post-layout analysis enables you to get the most accurate picture of signal quality – be it reaffirmation that signal reflections are within specified tolerances or a detailed check to ensure strict EMI standards are met.

If you analyze your signals prior to and after board layout, and check constraints as part of the pre-manufacturing DRC, you can be pretty confident that the only ringing will be the telephone, with a tender for your next project.