

Build 6.4.0.7263

PCB

- Octagonal pads are now rendered correctly when using Direct X graphics.
- Multi-trace routing now displays connection lines.
- Multi-trace route finishing angle, as toggled by '\ key, is now relative to the last tracks rather than absolute.
- The behaviour of the print dialog has been improved. It is now possible to re-order printouts and layers as well as multi-delete and insert them to a particular position.
- The Drag Room and Copy Room Format commands have been improved and now treat free pads the same as vias.
- Canceling drags of non signal layer objects no longer causes instability problems.
- Preserve angle drag feature has been improved. It now prompts before shifting locked objects and no longer creates duplicate tracks. It also correctly ignores pullback primitives on internal planes.
- Smart dragging has been enhanced and now handles collinear tracks in an appropriate manner.
- Background colored rectangles will no longer appear when scrolling with the mouse wheel whilst using GDI graphics.
- Ctrl + Drag no longer leaves tracks selected.
- The BOM output has been improved. Now the footprint names that contain only digits will no longer have the front zeros trimmed when Excel thinks that the string is a number.
- The Tracks Slicer command has been improved. Now the snap to grid works for vertical tracks as well.
- Improvements have been made to the Fan-out of Selected Components. Fan-out will only be done with the selected components, not all components on the board.
- Copy Room Formats command now copies the designator/comment TrueType font properties as well.
- The text object rotation handle will be correctly drawn at high-zoom levels or it will be removed entirely if the text object is deselected.
- Rotated slot blowouts on internal planes now draw correctly when using DirectX graphics.
- When using DirectX mode the Pad/via hole can now be turned OFF if needed, similar to the GDI mode.
- The drawing performance of the Select Connected Copper Command has been improved when using DirectX graphics.
- The Board Information Report has been improved. Slots and Square holes are now reported separately.

- Snippet drawing is now working correctly. The thumbnails will now be drawn as required.
- The Spectra DSN import from P-CAD into Altium Designer 6 has been improved. Now the Keepout regions inside components are imported correctly. The position of regions is now relative to the component that owns them not the board.
- The Arrange Components Outside Board command has been improved. Now it arranges the selected components based on the board outline or if this doesn't exist, based on the tracks present on the Keep-Out Layer. If no tracks are found on this layer then it behaves like before.
- The NC Route output for slotted pads has been improved. The G93 command that wasn't recognized by certain routing machines has been removed.
- Selecting masked out objects will now show the object alpha-blended with the selection rectangle so the user will be able to see what was selected.
- Hitting Escape when interactively editing the baseline, datum & leader dimensions will now revert back to the previous state of the object.
- Cut & Paste of a group of components from the PCB Editor into PCB Library Editor has been improved and no longer crashes.
- The designator/comment hide/show behavior has been improved. Now the designator/comment will hide/show when the corresponding flag is changed. This means there will be no need to redraw the entire PCB or move the component.
- The NC Drill Output has been improved. No buffer overrun exception will be generated, when long names are used, for the PCB document for which the NC Drill output was generated.
- The fan-out command has been improved when run on BGA. Optionally the outer two rows of the device can now be included in the fan-out.
- Hatched polygons using the Surround with Octagons option now pour correctly around vias. The vias will now only be outlined with octagons.
- The assignment of file extensions to Gerber files has been improved. File extensions are now assigned based on the layer's physical position in the stack-up.
- The fan-out of BGA components has been improved. Now if the Fan-out Style that the user chooses is BGA (selected in the Fan-out Design Rule) then the component will be recognized as being a BGA & the fan-out will follow this pattern. Now the users will be able to fan-out BGAs with less than 10 rows.
- The display of violating components has been improved. Now if the component has cleared the violation flag the same will happen with the designator/comment fields that sometimes remained in violation.
- The Tracks Slicer tool has been improved. Now it works correctly with the ALT key (when any Angle mode is used) if the start & end points of the Slicer are on the current grid. Note: if the start & end points are not on grid the Slicer ignores the ALT key.
- In DirectX Dimensions, selected drawing has been improved. Now the selection and the editing handles are shown. Also, the editing handles will be drawn non alpha-blended so they are easily visible.
- The NC Drill output from PCB has been improved. Now it generates correct data if the design contains vias & slots that have the same hole size but no round hole pads with the same hole size as the slots & vias. Also if the design contains

blind/buried vias then no drill files will be generated anymore for square/slot holes for other drill layer pairs other than the TopLayer:BottomLayer one.

- The Gerber Output of aperture macros has been improved. Now Oval pads that have $xsize < ysize$ will be correctly exported so any other CAM tool apart from CAMtastic will be able to load them correctly.
- PCB Layer Sets have been improved. Now the user will be able to save any user defined layer sets & load the saved layer sets into a new PCB. This way the user can reuse already created layer sets.
- The DRC report has been improved. Broken net violations caused by unplated pad are now only reported if the net is physically broken. Previously all unplated pads would cause a broken net warning to be issued.
- Board outlines containing arcs are now drawn correctly.
- Using Alt to temporarily disable the Avoid Obstacle option in the manual router does not try to snap the cursor to nearest 45 or 90 degree direction.
- Libraries are saved in version 5 using correct extension (PCBLib).
- After restoring shelved polygons online DRC is run.
- Name changes and pour order changes in the polygon manager dialog are propagated correctly.
- Hatched polygons now generate correct thermal reliefs in pads whose rotation is not whole number
- Inside PCB libraries, the Pad properties dialog focuses by default on "Designator" as it was done in Protel 99SE.
- Autoroute Connection does not cause intermittent crashes nor does it route the wrong connection.
- Thermal reliefs on solid polygon pours no longer cause clearance violations
- Paste masks in DirectX mode are now drawn correctly when negative override values are used.
- Cycling available connections using Ctrl+Space in manual router no longer causes an access violation.
- Single layer mode behaves correctly when the PCB panel is active and set to split planes mode.
- Previous version compatibility warnings are not displayed anymore when auto-saving a design.
- Thermal relief tracks no longer cause violations when hatched polygons are poured.
- Internal and split planes are now correctly highlighted in DirectX graphics mode.
- Board layers and colors dialog now uses the correct layer stack ordering when display is limited to layers in layer stack.
- Electrical grid now snaps to any angle tracks.
- The calculation of differential pair uncoupled lengths has been significantly improved.
- Version 5 PCBLibrary now saves in correct file format as specified by the user, instead of defaulting to Altium Designer 6.
- Hatched Polygons now obey clearance rules scoped with InNamedPolygon.
- Description of hidden objects is not displayed on the status bar anymore.

- The interactive routing dialog (invoked while routing manually) has been improved. Issues when clipping values incorrectly were resolved and operation was made more logically consistent and straightforward.
- Removing teardrops no longer causes net disconnection.
- Polygon manager now handles polygons on all layers except internal planes.
- In the interactive routing dialog the following issues have been corrected:
 - Reporting that typed impedance values are outside allowed range.
 - Spelling of the word 'impedance' (was impedence)
 - Width mode was previously always forced to 'user preferred' when closing the dialog.
- DirectX display now properly updates after changing the layer visibility for any layer other than the current layer from layers dialog.
- Pressing N while moving objects now updates displayed connections properly.
- An intermittent crash caused when unlocking workstations and using DirectX graphics has been resolved.
- Editing complex split planes through the layer stack manager or split plane editor no longer causes access violations or application lock ups.
- Align Horizontal and Vertical Centers are now functioning correctly.
- Selected Split Planes are now drawn correctly when using DirectX graphics.
- The arrow keys now work correctly for editing when using DirectX graphics.
- The DRC no longer incorrectly reports warnings and Broken Nets on unplated pads that have no hole.
- Plane splitting primitives are no longer randomly highlighted when selecting splits from the split plane editor.
- Visibility of connections is now correct when using DirectX graphics
- Layers using pure black as the color now hide correctly when using DirectX graphics.
- Situs no longer displays connections of nets associated with an internal power plane heading toward the origin of the workspace when using DirectX graphics.
- The arrow keys now function correctly when the system is initialized with GDI mode graphics.
- Character spacing in true type text no longer appears incorrectly when using DirectX graphics.
- The PCB editor has been improved. Dimension arrow lengths can now be edited regardless of the arrow position.
- Having a global (default) via with a start or end layer, not existing in the current board, no longer causes an access violation.
- Embedded board arrays are no longer obscured by the board into which they are placed when using DirectX graphics.
- Polygons without any associated copper, such as when the Remove Dead Copper option is on and no connection is made, are now drawn as an outline when using DirectX graphics.
- Version 6 Library files with a .Lib extension now correctly load into PCB instead of attempting to load in Schematic.

- Fonts changed from true type to stroke that have the inverted property set now draw correctly when using DirectX graphics.
- Internal planes in DirectX mode are now only drawn when they are the current layer. This is in line with the current GDI behaviour.
- An issue in the undo system causing incorrect pad rotations has been resolved.
- The Layer Stack-Up legend now draws correctly when being placed and when using DirectX graphics.
- Place Polygonal Room now displays correctly when using DirectX graphics.
- The birdseye view at the bottom of the PCB panel now functions correctly when using DirectX graphics.
- The display is now correct when redefining polygon vertices and using DirectX graphics.
- Component bodies are now drawn correctly when using DirectX graphics.
- When using DirectX graphics, moving or editing pads, vias and arcs no longer leave 'ghost' images on the screen.
- The Insight Lens now correctly tracks the windows mouse cursor rather than the snapped PCB cursor location when using DirectX graphics.
- Global changes involving true type fonts no longer cause an out of resources error.
- The display now correctly refreshes after changing layer sets when using DirectX graphics.
- The redefine board shape command is now functioning correctly when using DirectX graphics.
- The screen is now redrawn properly after deleting group objects in DirectX mode.
- The drawing of selected fills and rectangular pads has been improved when using DirectX graphics. The border width is now consistent on all sides.
- Keepout Fills, Arcs, Regions and Tracks that do not reside on the Keepout layer are now displayed correctly when using DirectX graphics.
- Connection lines (ratsnest) colors are now correct when using DirectX graphics.
- Multi-trace placement no longer places duplicate tracks.
- The STEP exporter has been improved to use object replication leading to reduced file sizes and load times into MCAD applications.
- A favorite via system, similar to the existing favorite track widths, has been added to PCB. This feature allows quick choice of the current routing via from a list of user defined favorites.
- The IPC Footprint Wizard now includes a generator for SOP (Small Outline Package) footprints (also includes SOP, SSOP, TSOP, and TSSOP).
- The IPC Footprint Wizard now gives a choice of pad shape; rectangular or rounded, for the SOIC, SOP and QFP footprint generators.
- The AutoCAD exporter has been improved. Vias are now exported to all relevant layers.
- Changing layers with the mouse wheel whilst in single layer mode now functions correctly when using DirectX graphics.

CAM Editor

- The DXF export from CAMtastic has been improved. Now the thermal definitions are exported correctly & the DXF file loads correctly in P-CAD 2004 or later.

Schematic

- When connection to an SVN repository using the SVN authentication, a dialog will be shown prompting you to enter your username and password.
- The Update from Libraries dialog has been improved:
 - On the second page, rows are now correctly reordered when the 'Update' checkboxes are checked on or off.
 - When choosing a new component from the second page of the wizard, the component selection in the page remains displayed.
- Copying of objects has been improved: An exception no longer occurs when repeatedly copying simultaneously unlocked component pins along with other objects on the sheet.
- The Place Part dialog has been improved: new comments typed in the 'Comment' edit box are taken into account when the OK button is clicked.
- Special strings have been enhanced: it is now possible to display a components current footprint name on the schematic by adding a parameter with a '=CurrentFootprint' value to the component.
- Copying components placed components back into a schematic library has been improved. The Footprint setting is now properly reset so that once placed, the footprint does not appear as though it is coming from a SCH library.
- Print preview mode for simulation charts has been enhanced. The following options have been included in the print preview page setup to allow customers to further customize their charts before printing:
 - Show Chart Title
 - Show Plot Title
 - Show Axis Labels
 - Show Data Points
 - Show Designation Symbols
 - Bold Waveforms
 - Highlight Similar Waveforms
- In Update from libraries, on the second screen, the All On and All Off menu options now work on the column you have selected. Selected On and Selected Off have been added to the menu. When you don't click on a column, the popup menu will show these options for all columns.
- The Schematic Library saving process has been improved. Component library references and aliases can now contain the (!) character.
- The schematic Copy command has been improved. Copying and pasting to Word no longer results in a clipped image.
- The schematic Jump Component command has been improved. Zooming now works correctly after this command has been executed, regardless of whether the mouse has been moved.
- The schematic editor has been improved. Part IDs are now displayed when designators are moved.

- The schematic library model editor grid has been improved. Components with added models now have their default models set correctly.

FPGA

- Placement of processors has been improved: the processor chosen in the Libraries panel is now correctly placed, removing the need to choose it again from the configuration dialog after placement.
- Support has been added for Xilinx® 8.2i.
- Fixed a crash when you Close All in the Devices View while having two or more projects open.
- Support for Lattice® ISP Lever 6.0 has been added.
- If the schematic sheet had a space or non valid VHDL character in its name and had a sheet symbol to a HDL sheet, Sheet Entry did not match to port and errors would incorrectly be reported. This has now been fixed.
- Support has been added for Actel 7.2 Designer/Libero.
- An improvement has been made to Nexus Manager to remove Nios® II from the Physical Device Chooser dialog.
- The FPGA->PCB wizard was not connecting bus ports properly from the sheet to the pins of the FPGA symbol in the auto-generated schematic sheet. This issue has been resolved.
- Fixed a bug where if there was noise on the JTAG chain the user would be presented with a lot of Power PC devices which caused a resource crash. The test to check whether there is noise on the JTAG chain has been made more stringent.
- Support for Lattice® MachXO family of PLD devices is now available.
- It's now possible to instantiate a black box in a VHDL or Verilog® file and has the system search for the EDIF models as it would for a schematic component. A new search option for pre-existing models for HDL documents has been added. This option is turned on by default.
- A new error check 'Check for Missing HDL Entity in Sheet symbol' has been added to compile. This error will check whether a corresponding entity that the Sheet Symbol refers to exists in the sub-sheet.
- Previously if you added a Generic device to the Devices View, the system crashed. This has been resolved.
- Several new core references have been added:
 - CR0165 VGA32_16BPP - 32-bit VGA Controller with 16bpp Data Support. This document provides detailed information with respect to the VGA32_16BPP peripheral device.
 - CR0164 Nios II 32-bit RISC Processor. This core reference includes an architectural description and on-chip debugging functionality for the Nios II processor family.
 - CR0167 WB_VGA Configurable Wishbone Display Driver. This document provides information on the configurable 32-bit VGA Controller peripheral.
 - CR0168 WB_MULTIMASTER Configurable Wishbone Multi-Master. This document provides detailed reference information with respect to the configurable Wishbone Multi-Master peripheral device.

- CR0166 VGA32_TFT - 32-bit VGA Controller with TFT Interface. This document provides detailed information with respect to the VGA32_TFT peripheral device.
 - CR0163 MicroBlaze 32-bit RISC Processor. This document includes an architectural description and on-chip debugging functionality for the processor.
- The existing core reference CR0113 VGA Controller has been renamed to CR0113 VGA - 8-bit VGA Controller. The information on the 32-bit VGA32 has been moved to a new document - CR0169 VGA32 - 32-bit VGA Controller.
- Several new application notes has been added:
 - AP0149 Allocating Address Space in a 32-bit Processor. This application note provides detailed information on mapping memory and peripherals into a 32-bit processor's address space.
 - AP0148 Connecting Memory and Peripheral Devices to a 32-bit Processor. This application note explores the various methods available for connection of physical memory and peripheral I/O devices to a 32-bit processor.
- The processor core reference for the PPC405A (CR0156 PPC405A 32 bit RISC Processor) has been updated. Information regarding connection of memory and I/O peripherals has been moved to the new document - AP0148 Connecting Memory and Peripheral Devices to a 32-bit Processor. Information on address space allocation has been moved to the new document - AP0149 Allocating Address Space in a 32-bit Processor.
- The processor core reference for the TSK3000A (CR0121 TSK3000A 32 bit RISC Processor) has been updated. Information regarding connection of memory and I/O peripherals has been moved to the new document - AP0148 Connecting Memory and Peripheral Devices to a 32-bit Processor. Information on address space allocation has been moved to the new document - AP0149 Allocating Address Space in a 32-bit Processor.

System-Level

- Closing an edited DBLink file and choosing not to save, no longer results in an error.
- Extracting sources from an IntLib now adds the extracted PCBLib as well as the SchLib to the newly created library package.
- The New Documents Defaults for PCB and PCBLib has been improved: new PCB or PCBLib documents added to PCB and Integrated Library projects are copied from the proper templates if one has been defined in Preferences>New Document Defaults.
- The search paths options dialog of DBLib documents has been improved: the dialog now processes relative paths correctly.
- Importing of OrCAD® database libraries has been improved: the OrCAD® CIS to DBLib importer no longer crashes.
- The word 'Protel' has been removed form the Search component dialog
- The PADS importer has been improved. Scope expression problems in clearance rules for polygons have been fixed.
- User is now informed if there are files in an output job that are no longer in the project.

- Confirmation has been added when deleting items; Double-clicking in an empty area creates a new item; "Show Completed Items" menu item persistent between projects and sessions.
- The P-CAD importer has undergone the following improvements:
 - The settings for minimum island sizes and the removal of unconnected islands in P-CAD copper pours are now imported.
 - All clearance attributes are now imported.
- The PADS library importer has been improved. Pad hole sizes are now imported.
- The OrCAD® MAX importer has been improved. Crashes no longer occur when importing library components with objects on internal plane layers.
- The library system has been improved. When placing a PCB component from an integrated library, the footprint library name is now set to the integrated library name, instead of 0.pcb.lib.
- The ECO generator has been improved. The status column is now included as part of the report.
- The P-CAD PCB importer has been improved. P-CAD layers will now be automatically mapped to an Altium Designer layer depending on their types.
- The following improvements have been made to the P-CAD PCB importer:
 - Polygon cutouts are now imported.
 - Imported layers are now automatically added to the layer stack and are enabled for display.
- The P-CAD library importer has been improved. Parameters are now imported into DB libraries.
- The library splitting process has been improved. Characters (*) and (") in component names are now dealt with correctly.
- The P-CAD importer has been improved. Footprint names will now be optimized depending on how many pattern graphics there are and whether the pad/pin mapping is simple. Symbols will also be optimized if the library is imported as a DB library.
- The design comparator has been improved. PCB rule directives in schematics will now match correctly to their counterparts in PCB.
- The Update from PCB Library command has been improved. Crashes no longer occur if the schematic components do not contain footprints.
- The OrCAD® MAX importer has been improved:
 - Unused layers can now be mapped to Altium Designer layers.
 - The "Invert Selection" command for layer mapping now works correctly when the grid is nested.
- The P-CAD SCH importer has been improved. Schematic files with NULL characters in them can now be imported.
- The schematic DWG exporter has been improved. Junctions are now exported without an arbitrary offset.
- The footprint manager has been improved. Components are now sorted in numeric order C1...C9, C10 and so forth.
- The OrCAD DSN exporter has been improved:

- Designators for multi-part components now contain the part designation (A, B, C etc).
- Port names are now positioned correctly.
- Single line texts no longer wrap around to become a 2-line text.
- Auto-junctions are now exported properly.

Embedded

- Simple example projects for Logic Zoom SDK boards fitted with LH79524, LH79520 and LH75401 have been added.
- An improvement has been made to ARM7 debugging to show all banked register values in the Embedded Register panel during debugging, and in the Nexus Debugger.
- An improvement has been made to correct a crash in the embedded project dialog when changing between memory spaces of an 8051 processor.
- An enhancement has been made in ARM7 support to support generic ARM7 devices. Any ARM7 microcontroller that adheres to the JTAG scan chain recommendations from ARM can now be debugged using the Altium Universal JTAG Connector.

Signal Integrity and Simulation

- Model file in the Sim Model properties dialog shows correctly and no longer as one single line when the default input language in Windows® Text Services and Input Languages are set to Hebrew.
- Signal Integrity has been improved. A source of access violation when the PCB pad count did not match the schematic pin count has been fixed.
- The Signal Integrity Model Assignments dialog has had the following improvements:
 - The value column for FPGA's is now updated correctly.
 - Changes in the Value/Type column are now propagated through to the Signal Integrity Model editor dialog when doing an advanced edit.
- Signal Integrity has been improved. The source of an AV when duplicate designator violations were present has been fixed.
- The Ibis Model Importer has been improved. It now imports models specified via the [Model Selector] keyword.
- Ibis Converter was improved. The correct filename is now displayed after importing an ibis file and the source of access violation during import of some ibis files has been resolved.
- OrCAD® PSpice simulation profiles are now imported including Transient, AC, DC and Sweep analysis setup information.