1. IPC Footprint Wizard now supports the following:
   - Molded Components - Capacitor, Inductor and Diode.
   - MELF components - diodes and resistors.
   - Precision wire wound inductors.
   - SOT 89 packages.
   - Dual Flat Pack (CFP) packages.
   - QFN packages with dual rows of pads equivalent to National Semiconductor's 128-pad laminated CSP package.

2. Fixed rare crash on PCB when OLD API used to access to Rules.

3. Fixed PADS importer - Keepout objects: Fix keepout object translation from PADS PCB ASCII to bring in using the correct layer. If the keepout object was set on "All Layer" in PADS, it will be put on a "keepout" layer in Altium Designer otherwise it will use the specific keepout layer. In the past, Altium Designer always puts the keepout objects on the "keepout" layer.

4. Enhance the PADS importer when translating PADS copper pour to Altium Designer copper pour. In the past, it only brings in the original copper pour outlines. It is now enhanced to also bring in the hatch outlines.

5. Fixed PADS Importer - Polygon objects: Fixed the PADS importer to correctly translate the polygon shape.

6. Layer stackup flipping in embedded board arrays has been improved. The signal and plane layers in the layer stack will be flipped together this will possibly allow you to flip a signal layer against a plane layer. This also allows you to have different layer types on the same layer on the embedded board array. The keyboard handling in From-To editor has been improved and we have added a new column Topology for Nets grid and Routed for From-To grid.

7. The IPC Footprint Wizard QFN generator now supports: LLP components with Power and Ground bars.

8. The IPC Footprint Wizard SOIC generator now supports SOIC components with exposed thermal pad.

9. Generating one mid layer in a PCB panel could generate multiple Gerber files: Now when generating only one mid layer from a PCB panel containing multiple embedded board arrays only one Gerber file will be generated.

10. PCB Layer tabs have been significantly improved. It is now possible to optionally use short layer names (Gerber Extensions) and display the layer color on the tab. From a right mouse click popup menu on the tabs, it is possible to access other layer related tasks such as highlight, show, hide, manage layer sets, layer stackup and drill pair.

11. A new interactive length tuning feature has been added to PCB. This provides a convenient way of adding addition length to existing routed traces. The style of the pattern used to add length is controllable and feedback is provided against any applicable length related rules. It is also possible to manually enter a target length.
12. DrillType keyword should no longer be accessible via the Filter Panel.

13. The IPC Footprint Wizard now has a batch mode that can read packages from input files (.xls and .csv formats), and generate footprints from this data automatically. Package input file templates can be found in the Templates folder in the installation directory.

14. When editing polygon vertices the cursor will no longer snap to itself allowing the expected movement on the current snap grid.

15. Multilayer pad clearances now calculated correctly against SMD pads.

16. A bug in the library reports has been fixed. The footprints are now visible in a library report if transparent layers are on in PCB display preferences.

17. The IPC Footprint Wizard incorrect footprint description and incorrect density level bug have been corrected.

18. The Gerber extension / ODB++ layer names in the Gerber / ODB++ Setup dialog will now appear in the order and with the names with which the respective layers will be generated. These names should match exactly the layer names and order that will be shown when the CAM data is loaded in CAMtastic.

19. Importing a DXF/DWG file into the PCB editor has been improved. Users now have more control over the position at which the file is located.

20. Improved usability of "Boards Layers and colors dialog". Visibility of each layer group in the dialog can be quickly changed independently of other groups.

21. Board level libraries have been added for Altera Cyclone III devices.

22. The IPC Footprint Wizard batch mode dialog box now has 2 buttons for loading blank template files included in the build, as well as view the template help for any of the supported package types. An option to generate all footprints into an open and active PcbLib file and the option to open all generated PcbLib files at the end of the batch process has been added. There is an alert for problems with input files when they are added prior to processing.

23. The IPC Footprint Wizard interface has been improved: On the first page it indicates clearly which component type to choose in order to create a given package.

24. A bug during the setting of the reference point for footprints created via the IPC Footprint Wizard batch mode has now been fixed.

25. The IPC Footprint Wizard now includes a generator for Transistor Outline (DPAK) components.

26. The IPC Footprint Wizard SOP generator now supports SOP components with exposed thermal pad.

27. The IPC Footprint Wizard now includes a generator for Leadless Chip Carrier (LCC) components.

28. In some cases when importing was carried out from the PCAD library the PCB Library file was empty: This problem has been fixed.

29. A new Stack-up Compatibility Report has been added and will flag any perceived incompatibilities between the layer stacks of the boards in embedded board array. Gerber and ODB++ generation for embedded board arrays has been improved; now embedded boards with different layers in their layer stacks will be exported correctly.

30. Board Level libraries have been added for Xilinx Spartan3A devices.

31. Pin swapping has been improved. Previously, if any component was not linked to a schematic component, pin swapping was disabled. Now it is possible to use pin swapping for linked components, ignoring unlinked components.

32. Gerber Extension and Layer Name have been added to Gerber / ODB++ Setup dialog for single board output.
33. Board level libraries have been added for Stratix II GX devices.
34. New mode added to PCB panel which provides comprehensive navigation, filtering and editing of drill hole information for PCB design objects.
35. Board level libraries have been added for Xilinx Spartan3L devices.
36. The report generator for the IPC Footprint Wizard batch mode now includes all errors and warnings in the report, and a potential memory leak was also fixed.
37. Board level libraries have been added for Lattice ECP2/M devices.
38. Snippets in PCB - room definitions were not placed properly: This has been fixed. It is now possible to place rooms from snippets.
39. Impedance driven Width Rule rounding problems: Improved rounding accuracy for impedance driven rules when switching between imperial and metric units.
40. Mismatched layer names in Hyperlynx Export: The Hyperlynx Exporter has been improved. Layer names are now consistent throughout the exported hyperlynx files.
41. Phantom electric snap when moving selection: The Move Selection command has been improved. The electric grid no longer snaps to objects in the selection.
42. A duplicate "L" hot-key has been removed from the PCB Tools Menu.
43. The Rounded Rectangular pads corner radius field will now be exported when generating a PCB Library from a PCB document.
44. Gerber and ODB++ generation for embedded board arrays has been improved; now embedded boards with different layers in their layer stacks will be exported correctly.
45. The "Test DirectX..." button has been fixed to work, even when there is no PCB document open.
46. Three new buttons have been added to the PCB Show/Hide preferences enabling quick manipulation of the Final/Draft drawing mode status of visible primitives.
47. SPECCTRA - Make restoring shelved polygons optional. This applies when exporting to DSN shelved polygons as they will not be restored before you export.
48. Find Test Points: Improved behavior of the “find test points process” has been implemented.
49. Shelve Polygon options now appear on the right click context menu (when user's cursor is focused on polygon object).
50. Increased minimum component grid resolution from 5mil (0.127mm) to 1mil (0.0254mm) - previously it was not possible to move components to 0.1mm grid.
51. No longer will the "is not a valid integer value" messages appear when an invalid value is entered. Now the control will reset it to 0.
52. The “touches room function” has been rectified to work correctly on small overlaps on the top edge of a rectangular room.
53. Now the slots in embedded boards will export to NC Drill with the correct rotation if the embedded board is rotated.
54. Printouts use to have pre 6.6 drill legend instead of new table format, this has been fixed. Printouts now use the new drill legend table.
55. The IPC Footprint Wizard QFN package now supports two different pitches ie one vertically and one horizontally.
56. DSN Importer: Updated SPECCTRA DSN file format importer now supports new format revisions ie Allegro produced support files.
57. Gerber files: Gerber files that contain arcs will be correctly generated all the time. Prior to this change some arcs could've been exported as counter-clockwise (G03) even if the ends shown them to be clockwise (G02).
58. Components that contain bitmap references are now correctly saved in PCB3d library files.

59. Reuse drill symbols for same drill sizes on all legends. Now the drill symbols will be reused when blind and buried vias are present in the design.

60. Solid polygon pouring around fills follows clearance more correctly using rounded outlining.

61. The corner radius for rounded rectangular pad shapes can now be changed using the Inspector and List Panels. This is similar to all the other pad's properties.

62. The Size of the hole string symbols in the drill legend is now correct. The DrillDrawing Legend will display the correct Symbol when the HoleSize String Symbols is used.

63. Single Layer Mode can now be controlled separately for PCB and PCB Library using new combo box control on the Board Insight Display Preferences.

64. Copying footprints with the same name between open PCB libraries will now use the correct footprint instance instead of the first found footprint.

65. Slice Tracks feature update: In the PCB Editor, any tracks that belong to a component that are locked or the component itself is locked, will no longer be sliced. Please note: In the PCB Library Editor the current behavior will be maintained.

66. Embedded Board Array display: The DirectX graphics mode has been improved. Embedded board arrays are now drawn in front of the defined board area.

67. Implement dragging of arcs whilst maintaining connectivity: Arcs can now be dragged while conserving the configuration of connected tracks. This is a new behavior that operates with the Preserve Angle When Dragging option checked in Interactive Routing Preferences. When you select and drag at the mid handle of an arc that is tangentially connected to tracks at one or both ends, the arc is dragged in a manner that maintains connectivity with its adjacent tracks.

68. Anti-Pads were not exporting correctly to ODB++ when slot holes are used: This has now been rectified; the anti-pads (voids) on internal plane layers will export correctly to ODB++ when slot holes are used.

69. Polygon cutouts to apply to polygons on non signal layers: Polygons placed on non signal layers will now obey cutout objects allowing more complex shape definitions on mechanical and overlay layers.

70. Component (CMP) records in ODB++ where previously missing part name. This has been fixed: the component records in the ODB++ component files will now contain the <part_name> = Component Comment (instead of the "???"). The comment should be unique and is used in the BOM to group the components so it actually behaves like a part_name. In addition, if the Comment contains spaces, these spaces will be replaced with '_' because Valor can not handle spaces in string literals.

71. SPECCTRA – would previously not run update free primitives when importing RTE File. After importing RTE File from SPECCTRA electrical primitives will no longer be updated from component pads, preserving their net assignments from SPECCTRA.

72. Missing micro vias in ODB++ output. There should be no missing vias in ODB++ drill files export if the vias have reversed start and stop layers.

73. Unions containing locked components could move without warning. Now a union that contains locked components will not be able to be moved. A message dialog will pop-up asking if the user wants to move the union regardless.

74. The PCB3D viewer has been improved in its support for different pad shapes. The viewer supports the rounded rectangular shape as well as the square and slot holes.

75. Background color for pcb3dlib. The background color was not working for pcb3dlib. This has been fixed.

76. ODB++ eda/data file now contains the net $NONE$ as the first defined net including all objects that have no net assigned to them.
77. DXP hangs when deleting excessive number of primitives from Undo Stack: Large entries in the Undo stack no longer cause delays when the undo limit is reached.

78. The stability of the undo system has been improved. Previously undo a delete operation had some potential to cause crashes at a later point in time.

79. Pouring a solid polygon over a multilayer pad with no land or hole size on the polygons layers no longer causes a void in the polygon.

80. Power Plane connection style now defaults to "No Connect" when no connect style rule is applicable to a pad or via. This behavior is now consistent with Gerber generation. Previously it was possible to have a clean DRC, but generate Gerber with connectivity problems due to plane isolations.

**Schematic**

1. A rare crash in Schematic on Altium Designer exit has been fixed. It no longer crashes when closing Altium Designer.

2. Port Cross Reference redrawing has been fixed. Port Cross References now display correctly in the schematic editor as the view changes.

3. Schematics have been improved. Designators can now be set so that they can be manually positioned.

4. During pin placement in Schematics an option has been provided that will allow the auto-increment feature to remove leading zeroes.

5. Unpredictable behavior while placing and modifying Bezier curves has been fixed.

6. Default primitives Permanent option: The Schematic component default is no longer modified after drag-n-dropping a part from the library panel, when the Permanent option is set to ON.

7. The paste tool has been improved. Previously, any transformations on clipboard objects during a paste operation were remembered in subsequent pastes. Now, subsequent paste operations use only the original clipboard objects, preventing unexpected changes.

8. The use of the Y key when pasting has been improved. Now, when pasting or dragging a selection of objects, the Y key will flip the objects including net labels with the correct orientation.

9. The function of reference zones in the margins of a schematic sheet has been improved. With "Show Reference Zones" turned off in the Document Options, the margins of the sheet now behave as any other part of the sheet. This makes it possible to click and drag to select objects at the border of the sheet.

10. The Schematic Inspector has been improved. Objects containing lots of parameters will no longer crash the Inspector.

11. The redirection text for the variant name, ‘=VariantName’, has been added to the list of parameters in the text properties dialog.

12. Place graphic - proportion was occasionally incorrect when first placed, this has been rectified and now when placing images on the schematic it respects settings in X:Y ratio.

13. Variant parameters are now supported in outputs. Add a variant parameter to 'Variant 1' (ie Name='VarTitle', Value='Title for Variant1'). Place a redirected text string with the format ‘=ParameterName’ (ie ‘=VarTitle’). At output, the parameter's value for the selected variant will be displayed (ie 'Title for Variant1').

14. Standard ASME Y14.1, calls for zone indicators to be alpha on the sides starting from the bottom working upwards - numeric on the top and bottom starting from the right to left. This update allows these zones to be specified in the template. Ensure the Port Cross Reference features work with the zones. Support has been added for the ASME Y14.1 sheet reference...
zone standard. In the Document Options dialog, make sure 'Show Reference Zones' is checked. From the drop down list below the check box, choose a reference zone style.

15. Schematic documents with rotated dot symbols can now be opened.

16. In the past, Altium Design will crash upon exit after importing P-CAD library file. This has been fixed.

FPGA

1. An automatically generated SDC file is no longer contains a comma as the decimal point for clock constraints. Commas were causing the constraints to be ignored by Actel while using non English language settings in Windows.

2. DSF drivers have been included for the WB_UART8 core.

3. Support for Altera Cyclone III devices has been added.

4. Support for Lattice ispLEVER 6.1 has been added.

5. Selecting an Altera Lead Free device is no longer causing the Build stage of the FPGA flow to fail with an Illegal Part Name error.

6. QuartusII and NiosII v6.1 Support: Support for Altera QuartusII and NiosII has been added.

7. Add JTAG sequences for Cyclone2 devices: Programming Altera Cyclone2 devices is no longer causing the "Failed to program device" dialog to popup after checking the Config_Done.

8. Default comment identifier for Altera TCLQ constraint file has been corrected.

9. Exception in CoreGenerator.Dll when synthesizing: Synthesis process for Actel cores has been improved to address an exception in the CoreGenerator module.

10. The document CR0122 EMACx Controller.pdf has been updated to fix incorrect register address representation. These addresses are now in true hex representation. Additional information has also been added for buffer and Controller initialization.

11. The Default Options button in the Error Reporting tab in the ProjectOptions for FPGA/CORE projects now sets all the error conditions to their correct default values.

12. It's now possible (added as an option called "Import All Signals") to include signals from a constraint file that are not part of the project. Previously the only way to do this was to open the constraint file outside of the project and do the import.

13. Mixed design (VHDL and Verilog) projects should now work properly when using XST as the synthesizer. Also search paths are now properly passed on for Verilog files.

14. Support for Spartan3A devices have been added.

15. Actel Designer 7.2 SP1 and SP2 are now supported.

16. A new core Importer Wizard has been added to assist in using third-party models from FPGA Vendor tools such as Xilinx's CoreGen or Altera's Megawizard. Just run the respective tools as standalone and then invoke the wizard via Tools -> FPGA Third-Party IP Import to use it in your FPGA project.

17. Programming support for Stratix II GX: Support for Stratix II GX devices has been added.

18. Programming support for Spartan3L: Support for Xilinx Spartan3L devices has been added.

19. Support for Xilinx ISE 9.1i has been added.

20. Programming support for ECP2/M: Support for ECP2/M devices has been added.

21. Third Party Vendor Tools Options has been upgraded to now support more options for all the vendors. There is now a feature to show/hide more advanced options.
System-Level

1. Advanced line numbers in the text editor: The text editor can now show numbers not for all lines but for every 10th one and for the current one. This significantly reduces information pollution and helps the eye to catch the crucial information.

2. A bug in the library panel has been fixed. An error that could occur when hiding the library panel after performing a library search has been fixed.

3. The library queries have been improved. A bug that raised an access violation when clicking ‘Edit PCB3D Model’ or ‘Edit Component’ from the query results has been fixed.

4. Sometimes the 2 Grids on the same form with Registry Path don’t store themselves correctly and overwrite each other. This has now been fixed.

5. Now if users close a HTML document from Free Projects it will always be correctly removed from Free Projects.

6. Now Font Dialog always appears on screen with an active window.

7. The SVN revision list now shows all revisions for files instead of only the revisions up until the checked out revision.

8. Variants have been improved. The problem with component variants losing their fitted/not fitted status has been resolved.

9. Support has been added for the SSH protocol for CVS.

10. The Pads Importer has been updated to now handle Pads Logic and Pads PowerLogic Schematic ASCII files. The versions supported are V2005.0, V2005.2 of Pads Logic, and V5.0, V5.2 of Pads PowerLogic.

11. The libraries panel has been improved. Libraries can now be activated and deactivated. In practice, deactivated libraries are treated as if they have been uninstalled by the rest of the system. Libraries can also be specified by using relative paths.

12. Basic version-control support for MatrixOne has been added.

13. Altium Designer no longer reads obsolete settings from the registry.

14. For CVS and SVN all calls to the version-control executables are now logged into the Output panel. This feature can be turned off through a preference.

15. Help buttons (with a question mark) have been removed from all wizard captions.

16. Delphi script was behaving incorrectly: Delphi script now correctly restores script state after a script exception.

17. A crash in the script editor when a script form contains a TListView has been fixed.

18. Now Browse Libraries saves the splitter position and size of all grid columns.

19. Now after you performed a View Desktop Layouts Default, all of the panels will be restored to their default positions.

20. Altium Designer will now always open maximized if it was closed maximized.

21. The accidental crash which was experienced when editing renamed .c files has been resolved.

22. Library report - Color option now always outputs color images: The Use Color checkbox when creating a library report is now checked by default. If the box is unchecked, footprints are still displayed in color, but the pads are drawn in draft mode for clarity when printing without color.

23. Incorrect hierarchy level for sub-sheets: The projects panel has been improved and the problem with displaying the structure of several sheets being referenced by a single sheet symbol has been resolved.
24. Tool bar positions are now saved properly in between Altium Designer sessions.
25. The bug encountered when linking a newly created Embedded project to an existing FPGA project has been fixed.
26. Access Violation when executing a process from toolbar: The launching of processes from a toolbar button has been improved. There is no longer an exception if the parameter string exceeds 1024 characters.
27. Select PCB Components dialog are sometimes too long: This has been rectified so that now when user selects Tools|Select PCB components only first 25 components specified and 3 periods added to avoid huge dialogs.
28. When documents are closed using CTRL-F4 the storage manager now correctly refocuses the view.
29. The choose columns dialog in the List panel for schematic and PCB is now resizable.
30. The crash experienced when minimizing, restoring and pressing the F1 key has been resolved.
31. The license usage information has been added to the 'Help, About' dialog.
32. Version control has been improved. A new batch commit command has been added so that all modified project documents can be checked in an atomic way.
33. Script documents are now flagged as modified after any form property has been changed.
34. The PADS Importer has been enhanced to handle PADS ASCII libraries. PADS Part libraries ".p", and PADS CAE decal libraries ".c" are translated into Altium Designer Schematic libraries, and PADS PCB decal libraries are translated into Altium Designer PCB footprint libraries. Versions supported V5.0, V5.2, V2005.0, and V2005.2.
35. SCH system menu - is sometimes not displayed: In some rare cases the SCH button at the bottom right of the screen did not appear.
36. Database libraries have been improved. Refreshing database libraries from the libraries panel now works correctly.
37. A bug in "Save Copy As" has been fixed. It is now impossible to "Save Copy As" over a file that is already open.
38. The PCB print properties dialog has been improved. The "Print Area" options now obey the unit system in the PCB.
39. A problem with closing the wrong project when attempting to close a non-saved project has been fixed.
40. Altium Designer now supports reading of PADS PCB files up to version 2005.2.
41. The P-CAD importer has been updated: it is now unnecessary to convert design and library files to ASCII prior to import. P-CAD Binary files can now be imported directly into Altium Designer.
42. A Print preview dialog crash under Windows Vista has been fixed.
43. When a project is created from a template containing external files (such as .Doc files), these files are no longer automatically opened separately when the project is created.
44. Now Altium Designer can import OrCAD® MAX files from read only files.
45. SmartPDF has been improved. A display of variant information in flat/global designs is now enabled.
46. The Libraries Search now has a new Simple search type. In this mode we can always search by entering a substring.
47. Library management has been improved. The user can now seamlessly switch between database libraries, integrated libraries, and source libraries (PCB and schematic libraries) by controlling how the library and tables names (if applicable) are taken into account.

48. Dragging component from Libraries panel to schematic or PCB document no longer causes an intermittent crash.

49. The icon in the projects panel has been updated to change from tick to exclamation mark to indicate 'Out of Date'.

50. In the past, the CircuitMaker 2000 importer did not bring in the input/output connector devices to Altium Designer schematic document. It has been fixed to convert the input/output devices to Altium Designer schematic ports.

51. Circuit Maker importer was not adjusting to the workspace size. This occasionally caused some items to be out of the schematic sheet border. This has now been fixed.

52. The order of sheets in Smart PDF has been improved. Schematic sheets are now ordered based on Hierarchical Structure then on sheet number. Sheet numbers can be set through Tools>Number Sheets.

53. Home key in text editor now behaves like in Visual Studio. It now jumps to the first non-space character on the line. The second home key will jump to the beginning of the line.

54. Added Window Vista support for updating of Altium Designer.

55. When printing from Print Preview in PDF Creator, all pages are now included in a single PDF File.

56. Replace network license term to floating license: In this version we are using floating license instead of network license.

57. The PADS importer has been improved. Single-layer pads and blind and buried via diameters are now imported properly.

58. OrCAD® Importer now correctly handles hierarchical blocks that are mirrored, so that the sheet entries are oriented and located correctly.

59. Closing the application when the library management homepage is open and focused no longer causes a crash.

60. Snippets - sometimes thumbnails were not visible immediately. This has been fixed with updating images when Snippet panel pinned and collapsed.

61. Parametric Hierarchy of User-Defined Net Classes: Net class generation has been improved. User-defined net classes can now be defined as a parametric hierarchy.

62. References - support opening word documents with component links: Now all components from Schematic support references to Word documents.

**Embedded**

1. Debug Search Paths for embedded projects: This is a new option in embedded project - Debug Search Path. Specify paths to directories, containing source code. This is useful for source files, which are not part of project, but implicitly included and compiled.

2. Issues with Memory configuration in Embedded Project options dialog: This has been fixed. 'Set to installation defaults' button in embedded project options dialog now correctly works for 'Configure memory' tab.

3. The generating error encountered when compiling an Embedded project if the code contained "#pragma message" has been resolved.
**Signal Integrity and Simulation**

1. The PSpice resistor has been improved. The Altium Designer parser now processes the PSpice temperature parameters correctly.

2. Print previewing charts has been improved. The number of plots per page are now displayed correctly.

3. The Voltage-Controlled Voltage and Current sources have been significantly enhanced. The PSpice 'FREQ' and 'LAPLACE' keywords can now be used with these devices. The FREQ parts are described by a table of frequency domain responses in either the magnitude/phase or complex number format. The LAPLACE parts allow the device characteristics to be described by a Laplace transform function.

4. SimView Import has been improved. Waveform names are no longer changed to lower case when a csv file is imported.

5. The Bipolar Junction Transistor (BJT) has been significantly improved. The BJT model extends the original Gummel-Poon model to include quasi-saturation effects, making the model compatible with the PSpice BJT model.

6. The Access Violation that was occurring if the Comment parameter was deleted or moved using the Sim Model Editor dialog has been resolved.

7. SimView print preview configuration has been improved. Print preview configuration can now be carried out from the "Default Prints" menu item on the Schematic or PCB menus without the system crashing.

**CAM Editor**

1. The Gerber Export has been corrected to no longer omit the end backslash from the folder name. This means the Gerber files will be generated in the selected directory.

2. Polygon cutout drawn last in CAMtastic using ODB++ output files will now show when loading ODB++ databases in CAMtastic, even if the Fill Mode is set to “ON”.

3. ODB++ - Duplicate FIDs found for duplicate tracks in PCB have been corrected. There should be no duplicate FIDs in the ODB++ eda\data file going forward.

4. ODB++ flipped components were incorrectly rotated, this has been fixed. Any flipped components rotated non-orthogonally will now appear with correct angles in Valor or any other application that loads the ODB++ data.

5. ODB++ - some of the FID entries in the eda\data file refer to wrong feature: Now no FID entries should refer to wrong features in the layers files.

6. ODB++ generate package contour from component bodies if they exist: Now the ODB package contour definition will be generated from component bodies if they exist otherwise the existing way will be used.

7. Special strings using Inverted text will be correctly exported to Gerber/ODB++.

8. ODB++ mid layer names not in order if the layers were swapped in layers stack: Now when generating ODB++ for a single board the mid layer names will be generated in ascending order similar with the Gerber output and the outputs for embedded board array.

9. ODB++ sometimes contours in complex polygons are not nested correctly: Now the complex polygons should appear correctly in Valor and there should be no longer any issues with the net list compare.