Prototype verification and debugging – reality bites

After months of developing your latest electronic product design using the best tools at your disposal, it’s reality time. The assembled prototype has arrived and is ready to be powered up for testing. All your careful development work, rigid design rules, SI analysis and pre-simulation passes will ensure that the prototype will work to specification with little chance of needing design revisions – what’s more, it even looks great.

The problem is, when powered up a major section just doesn’t work as expected. The next step is probably a spate of cursing, followed by a process of diagnosing and correcting the problem that will generally involve a gaggle of test instruments linked to flying probes or in a larger production environment, a bed-of-nails testing jig. This, coupled with the design documentation and your troubleshooting skills allows you to trace signals around the populated board to ultimately deduce the culprit.

Unfortunately this process has become increasingly difficult, thanks to the advent of extremely dense multilayer boards and the latest generation component packaging such as ball grid array (BGA) devices. With traditional testing and debugging techniques relying on physical access to key points and device pins on the board we have reached a point where this long-established approach is often unworkable or at best, inadequate. Indeed, where BGA-packaged devices are the main elements in a design, the inaccessible device pins make effective board diagnosis close to impossible.

Then there’s the added complication for development engineers resolving prototype errors. Unlike the process of faultfinding a previously-working unit that has developed a component or track-level fault, a prototype may also be crippled by a source design error, a board assembly problem or a board-level manufacturing fault. The design has never worked as such, so that frame of reference does not exist when diagnosing prototypes.

One solution to gain the required verification and debugging access is to include a large number of test points in your prototype board design, which expose all the key points and signal lines to your test instruments. Unfortunately, in larger complex designs this approach can have a significant impact on the board development time: its cost, complexity and physical size that may not justify the insurance of being able to access the prototype’s internals for troubleshooting purposes.

Removing the boundaries

In response to this disappearing pin access and the increasing density of new device packaging (typified by BGAs) test engineers formed the Joint Test Action Group (JTAG) in the late 1980s to address these restrictions by developing a new approach to testing, culminating in the Boundary Scan methodology (IEEE standard 1149.1) introduced in the early 1990s. Boundary Scan or JTAG-compliant devices include additional circuitry to create an embedded serial communication bus that can be programmed to capture then transmit snapshots of the logic state of all pins. Being a four-wire serial bus, the JTAG communications of all compliant devices can be easily chained in the board layout to facilitate final testing and debugging via a suitable interface.

The potential therefore exists to comprehensively troubleshoot and verify the latest generation complex designs that use pin-inaccessible high-density devices by using simple software interrogation via a JTAG hardware chain. In turn, the proliferation of JTAG-compliant devices opens this cost-effective possibility to all new designs and in particular those based on large-scale programmable devices such as FPGAs, without the need to rely on physical probing techniques and external stimulation signals.
Given a high level of JTAG support within a design, logical faultfinding techniques can be used to eliminate possibilities then track down the source of the problem – be it a dry solder joint, shorted track, incorrectly orientated component or heaven forbid a design error.

Faced with a wide range of electrical or functional fault possibilities, boundary scan analysis can vastly decrease design verification and testing time by helping you quickly eliminate possible causes, while guiding you to the source of the problem. Even better, if that capability was an integral part of the system you use for electronic product development, working with a prototype would no longer be a disconnected and cumbersome step in the process of taking a design from concept-to-completion.

### Watching the action in real time

Altium Designer natively supports this approach to working with board assemblies through a sophisticated range of JTAG-enabled features that can communicate with suitably-equipped boards, in real time. This might be Altium’s own FPGA prototyping board – the NanoBoard – or any JTAG-enabled board via Altium’s Universal JTAG cable or through expansion connectors on the NanoBoard itself.

Once connected to the four-wire JTAG interface, Altium Designer can access the boundary scan devices on your own prototype board then display the pin state results live on your development PCs screen. Any JTAG-compliant device can be accessed by including a matching Boundary Scan Description Language (BSDL) file – supplied by the device vendor – providing you with a complete JTAG-based insight in the internal state of your prototype.

By including the standard BSDL file supplied with each JTAG device you have access to the pins on every JTAG device in your design.

![Generic JTAG Device](image)

How you choose to display this information will depend on you own preferences or the type of pin state information that will most help you. Altium Designer offers design document level access to pin states through schematic-based test probes that are simply dropped on to the circuit where the logic state of a JTAG-accessible line or bus is displayed in real time.

If your preference or area of concern is at a board layout document level, Altium Designer also features real time pin state monitoring at a device and connected track level. This is ideal if you suspect that a misplaced component or faulty solder joint is preventing signal transfer between the pins of a (JTAG) device, or indeed between devices, where connected tracks are highlighted in real time to represent their logic state.
Beyond point-monitoring at a document level, Altium Designer also features an enhanced JTAG device viewer window, capable of displaying the state of all pins of a device in real time. This live view of a selected on-board JTAG device presents a continuous tabular update of all pin states, plus a representation of the pin action on a matching device schematic symbol and PCB footprint. When diagnosing or verifying the operation of your prototype, Altium Designer’s real-time viewer delivers a wealth of live information that provides a probe-less view of the board assembly's internal signals.

**Interacting in real time**

While a standard JTAG chain is ideal for accessing the state of compliant devices and connections on a board assembly – its original function – it can also be adapted to a variety of higher-level uses such as a convenient in-circuit programming port for FPGAs and other programmable devices. Taking this to the next level, a further working group has developed the Nexus standard that harnesses the existing JTAG “hard chain” to create an additional “soft” JTAG chain that facilitates working with embedded microprocessors – the access to logic states then includes the programmed soft devices within the fabric of an FPGA.

Altium Designer leverages the Nexus standard by providing native-level communication with the embedded structure programmed in an FPGA to enable a new interactive way of developing electronic products – Altium’s LiveDesign methodology. LiveDesign and Altium Designer form a unified design system that allows you to interact in real time with reconfigurable hardware implemented on an FPGA platform using on-screen virtual test instruments and processor debuggers – plus of course the document and window-based pin-state monitoring enabled by the hard JTAG chain.
To read more about LiveDesign -- Altium's revolutionary new approach to electronic product development – see ‘Create and work ‘live’ with soft PCBs’ and ‘LiveDesign’ on the Altium website. Altium Designer makes LiveDesign possible by unifying JTAG communications at the platform level to provide sophisticated, real-time access into previously inaccessible elements of your design. Whether you use Altium's JTAG-enabled technologies to verify and debug prototype or production board assemblies, or to harness interactive design on a reconfigurable hardware platform, the opportunity exists to develop better electronic products faster and at a lower final cost.

**Further information links**

- See the [enhanced JTAG viewer](#) in action
- See [generic JTAG support](#) (applying BSDL files) in action
- See [LiveDesign](#) in action
- Read more about Altium's [LiveDesign-enabled NanoBoard](#) or see it in action [here](#)
- Read about [Third-Party Development Boards and Altium's Universal JTAG Interface](#)