Design Rule Checking (DRC) is a powerful automated feature that checks both the logical and physical integrity of a design. Checks are made against any, or all enabled Design Rules, and can be made online - in real-time as you design - or as a batch process, with results listed in Altium Designer's Messages panel and a (optional) generated report.

This feature should be used on every routed board to confirm that minimum clearance rules have been maintained and that there are no other design violations. It is particularly recommended that a batch mode design rule check always be performed prior to generating final artwork.

Design rules collectively define the constraints for a board, ensuring that target object remain within design requirements and tolerances. For more information, see Specifying the Design Requirements - Design Rules. For a detailed reference of all rule types and their constraints, see PCB Design Rules Reference.

Configuring the DRC

Configuration for design rule checking is performed in the Design Rule Checker dialog, accessed through the Tools » Design Rule Check command.
In the folder-tree pane on the left side of the dialog, each of the design rule categories, whose rule types can be checked, are listed under the **Rules To Check** folder. Click on this top-level folder to list all checkable rule types on the right side of the dialog. Alternatively, click on a specific category to list only those design rule types associated to that category. Use the dialog to enable/disable Online (where available) and/or Batch Mode checking for each rule type you wish to check.

Use the right-click menu to access commands for quickly enabling/disabling all rule types for Online or Batch DRC, or only those rule types that are used (defined and enabled for use in the design).
Using Online DRC

Online Design Rule Checking runs in the background, in real-time, flagging and/or automatically preventing design rule violations. This is especially helpful when interactively routing your board, to immediately highlight clearance, width and parallel segment violations. For a rule to be subject to the Online DRC, the following three requirements must be met:

1. The rule must be enabled. This can be done in either the PCB Rules and Constraints Editor dialog, by ensuring the Enabled option for the rule is checked, or in the PCB Rules and Violations panel, by ensuring the On option for the rule is checked.

2. The rule type must be enabled for online checking in the Design Rule Checker dialog.

Ensure that design rules you wish to have monitored by the Online DRC are actually enabled for use in the design.
sure that the rule type is enabled for Online DRC.

3. The Online DRC feature must be turned on. Do this by enabling the **Online DRC** option, on the **PCB Editor - General page** of the **Preferences dialog** (DXP » Preferences).

![Preferences dialog](image)

Ensure that the Online DRC feature is enabled.

If any objects are found to be in violation of an applicable design rule that is enabled for online checking, they will be highlighted in the main workspace, in accordance with defined **violation display options**.

**Using Batch DRC**

Whereas Online DRC only detects new violations - violations that are created after the feature is enabled - Batch DRC allows a check to be manually run at any time during the board design process. So while good designers know the value of Online DRC, they also know that board design should begin and end with a Batch DRC.

Enable rule types for batch checking in the **Design Rule Checker dialog** as required (refer back to **Configuring the DRC**). Various additional options are available when running a Batch DRC, including the ability to generate a report file. These options are accessed by clicking on the **Report Options** folder, in the folder-tree pane of the dialog. Two key options (highlighted in the following image) are:

- **Create Report File** - enable this option to generate a DRC report.
- **Create Violations** - enable this option to have violations highlighted in the workspace, in accordance with defined **violation display options**. This option is also required to have violations appear listed in the **Violations** region of the **PCB Rules And Violations panel**.
A batch-mode DRC is initiated by clicking the **Run Design Rule Check** button, at the bottom-left of the dialog. After the check has completed, all violations are listed as messages in the **Messages panel**. If you opted to do so, a DRC report will be created, and automatically opened (if configured to do so) as the active document in the main design window. The report lists each rule that was tested, as specified in the **Design Rule Checker** dialog. Rules that are not present in the design are not tested.

**DRC Reports**

Enabling the **Create Report File** option in the **Design Rule Checker dialog** will generate a DRC report upon execution of a Batch DRC. Options available on the **PCB Editor - Reports page** of the **Preferences dialog** allow specification of report format, and whether the report is automatically displayed after generation.
Generate a DRC report as part of the Batch DRC process.

Supported formats are:

- **TXT** - generates the file `Design Rule Check - <PCBDocumentName>.drc`.
- **HTML** - generates the file `Design Rule Check - <PCBDocumentName>.html`.
- **XML** - generates the file `<PCBDocumentName>.xml`.

TXT and HTML format reports are generated into the folder specified in the **Output Path** field, on the **Options tab of the Options for Project dialog**. The XML format file is generated into the same location as the parent project file.

The report lists each rule that was tested during the batch checking process, as specified in the **Design Rule Checker** dialog. Each violation that was located is listed with full details of any reference information, such as the layer, net name, component designator and pad number, as well as the location of the object.

In the HTML format report, click on the entry for an offending object to cross probe directly to that object in the workspace.
Violation Display Options

Checking the design against specified design rules is one thing, but what happens when one or more of those rule are violated? Whether running Online DRC during design, or manually running a Batch DRC, there needs to be some visual indication of where such rule violations are occurring. The PCB Editor includes powerful violation display options to indicate where violations exist in a clear, visual way.

Custom Violation Graphics

Most design rules that can be included in either Online and/or Batch design rule checking have associated custom violation graphics - appearing within the workspace when a particular rule is violated. These graphics provide a visually cleaner DRC landscape. When a particular design rule is violated, the associated custom violation graphics (where applicable) are only drawn on the layer(s) involved with that violation.

In some cases, the graphic shows not only where the violation is occurring, but also why - displaying the constraint value defined for the rule and indicating how the offending primitive(s) are either below or above this value.

Example illustrating the custom graphics used for width and minimum annular ring rule violations.

Other graphics, including those used to represent violations of Net Antennae, Short-Circuit, Room Definition, Layer Pairs and Vias Under SMD rules, will simply be a graphic, as there is no definable constraint value to be displayed.
Violation Overlay

In addition to the custom violation graphics, a violations 'overlay' is available for setup and use. The overlay draws over design primitives. You have a choice of what pattern to display on the primitives, from a selection of styles.

![Violation Overlay](image)

Use a violation overlay as an alternative to the custom violation graphics when displaying DRC violations.

Using a combination of the two violation display types can prove useful in terms of providing a 'coarse' and 'fine' indication of violations. When zoomed out, the violation overlay can flag where a violation exists, then zoom in to view the detail delivered by the associated custom violation graphic.

Configuring Violation Display Preferences

Control over how DRC violations are displayed - using the custom violation graphics and/or a defined violation overlay - is specified on the PCB Editor - DRC Violations Display page of the Preferences dialog (DXP » Preferences).
Configure how DRC violations are displayed in the workspace - using custom graphics and/or a defined violation overlay - as part of your Altium Designer preferences.

Options available allow you to:

- Choose the style of violation overlay used.
- Determine violation display behavior when zooming in and out. For example, determining the point at which the custom graphics for a violated design rule will be displayed.
- Choose the display style used, on a per-rule basis. Enabling the **Violation Details** option for a rule type will use the associated custom violation graphics to display the DRC violations of that rule. Enabling the **Violation Overlay** option will display the violations using the specified overlay style.

Right-click within the grid to access a menu of commands to quickly enable or disable use of a violation display type for all rule types. Commands are also available to quickly enable the display of violations - detailed graphics or overlay styles - for only those rules currently being used in the design.

**Defining Violation Coloring**

To give further flexibility when displaying rule violations in the workspace, the two violation display types - violation details (custom violation graphics) and violation overlay - have separate associated
system colors. This allows you to differentiate between the two using different, distinct colors. Color assignment is performed on the Board Layers And Colors tab of the View Configurations dialog (Design » Board Layers & Colors):

- **Violation Details** - uses the color assigned to the DRC Detail Markers system color.
- **Violation Overlay** - uses the color assigned to the DRC Error Markers system color.

Specify different coloring for the two violation display types, and enable/disable their display as required.

For the violation display type to be used, ensure that the Show option next to the system color entry is enabled, otherwise the associated violation details or violation overlay will not be displayed.

**Interrogating & Resolving Design Violations**

With care and attention, and staged design rule checking along the way, running that final Batch DRC on the finished, fully routed board, may yield only a few design violations, if any. However, there may be a sizeable quantity of violations flagged, and now the task becomes one of resolving those violations.

DRC reports generated by running a Batch DRC can appear quite daunting to the new PCB designer. The secret to keeping the process manageable is to develop a strategy. One strategy is to limit the number of violations that are reported. When setting up the report options in the Design Rule Checker dialog, set the Stop When Found feature to a small number. Another strategy is to run the DRC in a number of stages. If the design contains a large number of violations, begin by enabling the rules one at a time. With experience, you will develop a preferred approach to testing the various design rules.

To effectively resolve a design violation, you must first be able to locate it. The PCB Editor provides various methods for interrogating design violations, as described over the following sections.
From the PCB Rules And Violations Panel

When running an Online or Batch DRC, any rule violations will be listed in the Violations region of the PCB Rules And Violations panel. Browse violations associated with a specific rule class, or individual rule within a class. Alternatively, browse all violations by selecting the [All Rules] class.

When running a Batch DRC, violations will only appear listed in the Violations region of the panel provided the option to Create Violations is enabled in the Design Rule Checker dialog.

Clicking on a violation entry will apply filtering using the offending object(s) as the scope of the filter. The resulting view in the main design window will depend on the highlighting options enabled (Mask/Dim/Normal, Select, Zoom) at the top of the panel.

![Diagram showing PCB layer and violation highlighting](image)

interrogate rule violations using the PCB Rules And Violations panel.

Violations themselves - or the custom violation graphics to be more specific - are drawn only on the layer(s) involved in the rule violation (the layers on which the offending primitives reside). Clicking on a particular violation will cause the layer on which that violation is associated to become the active layer in the workspace, provided of course that the layer is enabled for display.

Double-clicking on a violation entry (or right-clicking and choosing Properties) will open the Violation Details dialog, which provides information about the rule being violated and the primitive(s) responsible. From this dialog the offending object can be highlighted (causing it to flash in the workspace) and jumped to, effectively providing 'zoom and center'.

Highlighting essentially leaves the offending primitives in their normal visibility, with all other objects in the workspace becoming temporarily monochromatic. It is therefore advisable not to have any masking or dimming applied prior to accessing the dialog, or to access using the right-click Properties command.
Using the Violation Details dialog to highlight the primitives involved in a design rule violation.

**From the Messages Panel**

After running a Batch DRC, double-clicking on a violation message in the Messages panel will cross-probe to the object(s) causing that violation in the workspace.
Cross-probe to a violation from the Messages panel.

To have violations displayed in the workspace after running a Batch DRC, ensure the option to **Create Violations** is enabled in the Design Rule Checker dialog.

### From a Generated DRC Report

If the option to **Create Report File** is enabled in the Design Rule Checker dialog, violations detected upon running a Batch DRC will be listed in a generated report file. Click on the hyperlinked entry for an offending object to cross-probe directly to that object in the workspace.

The offending object(s) will be zoomed and centered, but no other highlighting (masking, dimming) will be applied.
Cross-probe to an offending object from the generated DRC report.

**Directly in the Workspace**

Violations associated with a particular design object can be interrogated directly within the PCB workspace. Position the cursor over an offending object, right-click and choose a command from the **Violations** sub-menu. Either choose to investigate an individual violation that the object is involved in, or choose to view all violations in which it is involved, using the **Show All Violations** command. In each case, the **Violation Details dialog** will appear, providing detailed violation information and controls for highlighting and jumping to the offending object(s).
Interrogate violations involving a specific object directly in the workspace.

Violations can also be browsed directly in the workspace using the Board Insight pop-up. Simply position the cursor over an object in violation and toggle display of the pop-up using the Shift+V keyboard shortcut. Click on a violation entry to access a menu of commands, including Properties, which gives access to the Violation Details dialog. Expand an entry to browse the primitive(s) involved.

✔ Buttons for each of the Properties, Select and Zoom commands are also available to the right of a violation entry.
Interrogate a violation using the Board Insight pop-up.

Violations can also be browsed through the full Board Insight panel.

**DRC Validation in an Output Job**

Altium Designer provides the ability to define and run a DRC validation report as part of an Output Job Configuration file (*.OutJob). With an OutJob file open as the active document, the report is available from the Validation Outputs grouping of outputs. To add a report, simply click the [Add New Validation Output] control and choose the Design Rules Check entry, selecting the PCB document as the source.

To keep things non-specific, a generic entry for the underlying Data Source is available for selection - [PCB Document]. By keeping an OutJob generic, you can effectively maximize its ability to be reused across future design projects.
Add a DRC validation report to an Output Job file.

There is no separate configuration dialog for a Design Rules Check validation report. The checking is performed using the settings defined for the PCB document in the Design Rule Checker dialog.

**Validation as Part of PCB Design Release**

Using validation reports defined in an assigned Output Job file, Altium Designer provides the ability to validate designs as an integral part of its board design release process. These validation checks will be performed on every release, and the release will fail if any validation checks are not passed successfully. Validation is run at the Validate Design stage of the process flow within the PCB Release view.
Example of a successful validation stage being run within the PCB Release view.

For more information on using the PCB Release view to release your board designs, see Releasing a Design.

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