The PDN Analyzer application is relatively straightforward to use, and basically involves setting up the PI-DC simulation net/device parameters, running the simulation and then interpreting the results. The simulation can be re-run at any stage, which makes it easy to make changes to the PCB that may improve the power integrity of the supply paths, and then test the results.

This 'walkthrough' demonstration guide to working with the PDN Analyzer uses Altium Designer's supplied Spirit Level example project, which can be found in the software's documents folder – typically C:\Users\Public\Documents\Altium\ADxx\Examples\SpiritLevel-SL1, where ADxx represents the installed version of Altium Designer. This guide information assumes that the PDN Analyzer is installed and licensed in Altium Designer, and that you have a base understanding of the PI-DC (DC Power Integrity) principles used.

- See the PDN Analyzer page for information on installing/licensing the PDN Analyzer extension and also the basics of PI-DC simulation.

Note that the PDN Analyzer powered by CST® runs on Windows 64-bit systems only, and requires Altium Designer version 16.0 or above.

PDN Analyzer Interface

The PDN Analyzer extension's interface is invoked as an Altium Designer panel, which can be docked or floated in the workspace. To open the main PDN Analyzer panel, open a schematic or PCB document (in this case, from the loaded Spirit Level project) and select the application from the Tools menu (Tools » PDN Analyzer).
The panel's visual arrangement emulates the analysis circuit, in terms of source/load objects and supply/return paths, where the object blocks also provide information and data entry points. If all of the objects shown above are not visible, the panel may need to be resized.

**Panel notes:**

- Power and Ground Net objects with a dark gray background are editable.
- Power and Ground Net objects with a white background are not editable – other object blocks must be edited/supplied before these are enabled.
- Source or Load object blocks with a light blue background are editable or have been edited, and can be further edited if necessary.
- Source or Load object blocks with a light gray background are not editable – other object blocks must be edited/supplied before these are enabled.
- The **X** button associated with a Source or Load object clears the parameter entries for that object.
- The **save config** button allows the current PI-DC configuration to be saved (or resaved) as a nominated *.*.pidc_config file in the project's directory.
- The **load config** button allows a previously saved PI-DC configuration to be loaded as the simulation settings.
• The **save config as** button allows the currently active PI-DC configuration to be saved as a nominated *.pidc_config file in the project's directory.

• The **reset config** button clears the panel's current configuration entries.

• The **+** button adds a further Load object between the Power and Ground nets.

• The **Metal Conductivity** link opens the **Metal Conductivity dialog**, which displays the current net conductivity value and allows modification of base metal conductivity and temperature compensation values.

• The **Start Simulation** button (bottom left of the panel) instigates the PI-DC simulation process, and is only enabled once all required parameters have been provided.

• The panel also includes a Results mode that is enabled when a PI-DC simulation has been successfully run – this is opened from the **PDN Analyzer Result** tab at the bottom of the panel, and may be separately floated.

Three examples are included below to demonstrate using the PDN Analyzer, and how multiple loads and power networks are supported. After running and analyzing these examples, you should be familiar with setting up, saving, executing, and analyzing PI-DC simulations within Altium Designer.

**Example 1**

This demonstration example involves setting up a PI Simulation for the PCB supply path between the design's VCCINT rail (1.8V) and the U1 device as a load. It also covers the display and assessment of the Voltage Drop in both the VCCINT and GND net copper paths, and also the Current Density for those nets.

![Example 1 power source circuit](image)

**Step 1:** Open a schematic or PCB document of the Spirit Level project and invoke the PDN Analyzer extension from the **Tools** menu. The **PDN Analyzer** panel will open – If necessary, **Reset** the current configuration (**reset config**) to clear previously used settings.

**Step 2:** Click the panel's **<Source Power Net>** object box to choose the power delivery net from the pop-up source net dialog - select **VCCINT** for this simulation.
By default, the net dialog's filter options (at the top) are set to list only likely power nets. These are preset to accept:

- All types of net shape types (not just those connected to planes and polygons).
- Only nets that have 3 or more connections.
- Only nets that are named with a V prefix.

When all filter options are cleared, the dialog will list all available nets in the PCB design.

Note that after the Source Power Net has been selected (VCCINT) and the dialog dismissed (OK):

- The <Source Power Net> object displays the selected net.
- The <Loads Power Net> changes from a white to gray background, indicating that it is now editable.
- The supply Source object changes to a light blue background, indicating that it is also editable.
- The hint message associated with the simulation button changes.

**Step 3:** Ensure GND is already selected as the <Ground Net> (the panel's lower object box). If this is not the case, it can be selected in a similar way to the Source Power Net above. For this net selection, the dialog filters are preset to list only nets that have 3 or more connections, and are connected to planes and polygons.

**Step 4:** Select the Source object (labeled as <RefDes.Pin>) to choose the supply source, and its connections and parameters – in this case the 1.8V Voltage regulator, U4. The power source device
and (optionally) pins are entered in the Source dialog.

Use the dialog's PWR Component Pins drop down menu to select the power source – in this case **U4**. In this design, U4 does not have a direct ground pin connection (it’s essentially a current regulator), so **J1** can be selected as the Ground component from the GND Component drop down menu – note that pins 2 and 3 of the power input socket J1 are connected to the GND net.

Both the Source Properties and Load Properties dialogs provide an additional net component filter that will exclude capacitors (those with a ‘C’ prefix) from the Component listing. Select the **Hide C** checkbox to enable this filter.

Nominate a suitable voltage level and current capability for the source supply device. We’ve chosen to derate the 1.8V supply by 5% (or 0.1V) for a **1.7V** simulation source, and selected **5A** as the maximum current for the part and the current that each of its pins can deliver. Note that the Pass/Fail Criteria settings are optional and can be omitted if excessive current drawn from the Source is not of concern.

**Step 5:** Select the <Loads Power Net> object box, which opens a dialog similar to that used for the Source Power Net (above). This will default to the same net as the source power net (VCCINT), so the dialog can be immediately dismissed with the **OK** button.
The Load and Source power nets are now the same, so the panel's Power Net box becomes continuous (as VCCINT) - the message associated with the button will also change.

Select the Source object (labeled as `<RefDes.Pin>` ) to choose the supply source

**Step 6:** Finally, click the Load object box (labeled as `<RefDes.Pin>` ) and choose U1 as the Load Component and GND Component, and enter its load parameters (load current and minimum supply voltage). For this example it's assumed that all of U1's pins have the same parameters. If some pins had different parameters, only a subset of the pins would be selected and assigned parameters. Another, separate U1 load would then be added for the other pins, and assigned suitable parameters.

A minimum supply voltage of **1.6V** (allowing for a 10% DC drop; 1.8V - 10% = 1.6V) and a load current of **0.5A** has been nominated. Note that the Pass/Fail Criteria setting is optional and can be omitted if excessive voltage drop at the Load is not of concern.

Note that unit prefixes (for example, 500m to represent 0.5A) are supported.
Step 7: Following the successful configuration of the simulation, all the panel's boxes will contain valid parameter data – this is a good time to check that the entered parameters are correct in each object box. The message next to the button (which is now blue) indicates that the simulation is ready to be run.
Step 8: Click the **Start Simulation** button to instigate the PI-DC simulation and observe the process and results.

The progress of the simulation will show as a stream of events in the Messages panel, which will also indicate the cause of a simulation failure if the process is unable to complete. A completed simulation is indicated by the 'Simulation run successfully' status text associated with the **Start Simulation** button.
Note that the panel's Source/Load objects now shows current and voltage results for the source and load, respectively.

The source/load objects are shown with green 'success' check marks, since the pass/fail limits that were entered (when setting up the simulation) have not been violated - specifically, a maximum Source current of 5A has not been exceeded (0.5A), and the Load voltage is higher than the nominated 1.6V minimum (1.69V). A violation of the limits would be indicated by a red fail icon.

**Step 9:** The results of simulation can now be viewed graphically in Altium Designer's PCB editor. To see the Voltage (drop) results, select the panel's **PDN Analyzer Result** tab, and check the **Voltage** option in the **Display Filter** section of the results window. Set the view to the board's power net path by selecting **VCCINT** as the Net, and both the **Top** and **Bottom** Layers.
The analyzer results are displayed as a rendered overlay in Altium Designer’s PCB Editor, and the display can be set to 2D or 3D format with the **PDN Analyzer Result** panel's buttons. These buttons are equivalent to the **Altium 2D PDN Analyzer** and **Altium 3D PDN Analyzer** views in the PCB editor (as shown below). In general terms, the 3D option will provide a more thorough view of the board Layers and Vias, whereas 2D is a simpler (and therefore less cluttered) view.

With the 3D view option selected, the graphical representation of the simulation result will look similar to that below.
The view of the selected net path voltage drop, in this case VCCINT, is rendered with a color gradient that corresponds to the Voltage scale presented at the bottom of the view. By default, the scaling is set to automatically span the full voltage level range delivered by the simulation (see the panel's Results window for manual scaling options).

Note that in this example:

- The highest Voltage displayed on the scale is 1.7V (1.6995), which is indicated at the source (U4).
- There is no significant DC Voltage drop between U4 and the decoupling capacitor C3 (no current flow through an ideal capacitor).
- The lowest Voltage displayed is 1.69V (1.6871), which is shown at the load (U1).
- There is very little voltage drop (around 12mV) through the VCCINT power delivery shape when a load of 0.5A is assumed.

By viewing Voltages in 3D mode and panning the view, it can be seen that there is some voltage drop at the three vias (a difference in color between the top and bottom of the vias) and in the trace between U4 and U1.
**Step 10:** View the Current Density results of the voltage net (VCCINT) graphically. In the panel's Results window, select the **Current Density** option – and the VCCINT net and both Top and Bottom layers, as before. The above Voltage Drop image and the matching Current Density image below illustrate the situation where the design's Via size/weight is insufficient.

- See [Via Wall Thickness](#) for information on setting the DC performance of Vias.

Also notice that, beyond any limitation imposed by the Vias, the track between U4 and U1 has the highest current density and could be widened if the design needed to be improved.

Areas of high current density in the design are easily detected by taking an overall view of the board, which also includes a Current Density display graphic. The range of the displayed Current Density scale is automatically determined from the simulation results (the default **Auto Scale** option), and indicated in A/m² (amps per square meter) **by default**.
Step 11: View the Voltage results of the ground net (GND) graphically. In the panel's Results window, select the **Voltage** option, the **GND** as the Net and the **Top** Layer. Notice that there is very little voltage drop through the large GND shape – the maximum voltage is only 1.37mV.

However, if you switch the results mode view to **Current Density** and view the **GND** net (**Top** layer), a potential issue with the design can be seen. The view shows both 'peninsulas' and 'islands' in the GND shape, as indicated by their blue color (no current flow). Of course, this only represents the DC current flow for VCCINT, whereas all other DC voltages must be checked before it can be confirmed that these portions of the GND shape are in fact unused.

It is also essential to check that ground shapes are not used for AC current return before removing them, perhaps by replacing capacitors with 1k-ohm resistors in a simulation to view their impact on the return path. Nevertheless, it is clear that even small connections in a critical location (say, at the bottom left of U1) would convert the large GND peninsula to a less problematic ground shape.
In practice, these peninsulas and islands can cause problems due to AC and transient voltage characteristics, and should therefore be avoided. Power delivery shapes should ideally have connection points on all their major sides.

Another point to notice in this view is that the current flowing from left to right (as a ground return path) is limited to narrow strips above and below U1 in the design. If the total current traveling in this layer was significant, the narrow shapes would become a problem by causing the voltage on the ground plane to be significantly higher than the 1.37mV derived by the 0.5A simulation.

Viewing the ground shapes using the PDN Analyzer's Current Density display can provide valuable insights into a design's layout.

**Example 2**

This demonstration example involves setting up a PI Simulation for the PCB supply path between the design's VCCO rail (3.3V) and multiple load devices, including a resistive load and different pin loads of U1. The example uses the Spirit Level design supplied with the Altium Designer installation, and is run in a similar way to that outlined for Example 1.

The Example 2 power source circuit – see SL_Power.SchDoc in the Spirit Level project.

In the main *PDN Analyzer* panel window, save your current configuration using the (or ) button and then clear that configuration with the button.

Enter the following settings, using the panel's button to add additional loads as needed:
- **Power Net** (both Source and Loads): VCCO
- **Ground Net**: GND
- **Source**: U3.2 (Power Component), J1.2,3 (Ground Component)
  - 3.15V (3.3V – 5%) Source Voltage, assuming 5% derating
  - Maximum of 5A through source and all source pins
- **Loads**:
  - R20.2 (power), U6.3 (ground): representing the design’s Done LED
    - 270Ω nominal Load Resistance
    - 3V minimum Voltage (3.3V – 10%)
  - U5.18 (power), U5.11 (ground): JTAG VCCINT
    - 0.01A
    - 3V minimum voltage (3.3V – 10%)
  - U5.19 (power), U5.11 (ground): JTAG VCCO
    - 0.04A
    - 3V minimum voltage (3.3V – 10%)
  - U5.20 (power), U5.11 (ground): JTAG VCC
    - 0.05A
    - 3V minimum voltage (3.3V – 10%)
  - U1.* (power, use all available pins), U1.* (ground, use all available pins): FPGA 3.3V
    - 1.875A
    - 3V minimum voltage (3.3V – 10%)
  - R11.1 (power), U2.3 (ground): U2 current
    - 0.005A
    - 3V minimum voltage (3.3V – 10%)
  - R16.1 (power), S3.3,4 (ground): Y1 current
    - 0.012A
    - 3V minimum voltage (3.3V – 10%)

In the **Load Properties** dialog, the **Load resistance** value for a selected resistor component is automatically populated by information extracted from the PCB design.

When all entries and parameters have been added, the **PDN Analyzer** panel should appear as below:
Note that exclusively resistive loads cannot be simulated, and at least one current sink is required. If you wish to run an analysis on just the resistive loads present on a power rail, add one current load and set this to a very low load current value so its affect is negligible.

This example demonstrates:

- The ease of adding multiple loads to the simulation.
- The value of the panel's graphical representation of the simulation topology and data, which helps to ensure accurate entry of parameters.
- The ability to assign different current values to particular pins a load device (U5, in this case)

Note that resistors do not report voltage values, or the pass/fail status of those values compared to the entered parameters. This is a software limitation will be addressed in the future.

If you run the simulation and view the voltage on the ground plane in the PCB editor, there will be an indicated 5.3mV voltage drop on that plane. This is significantly more than the 1.37mV drop due to VCCINT (see Example 1), since there is a larger current through the VCCO net - both supply rails use the same ground plane, so the cumulative effects need to be considered.
Example 3

This demonstration example involves setting up a PI Simulation for the PCB supply path between the design's 5V power input (PWR_IN) to the 5V supply via an intervening device, and to multiple load devices including U3 and U4. Again, the example uses the Spirit Level design supplied with the Altium Designer installation, and is run in a similar way to that outlined for Example 1.

Here, the 5V supply (sourced from the PWR_IN net at the J1 connector) can be analyzed by selecting PWR_IN as the source power net and 5V as the load power net – you will need to deselect the dialog net filters to list the PWR_IN net. The PDN Analyzer automatically constructs the DC path between the two nets, including the intermediate net NetD1_2 (in the schematic, the upper pin of zener diode D1).
Note that the 5V supply path has been correctly constructed between the J1 input (PWR_IN) and the 5V supply, including the link connections of the Polyswitch (F1; pins 1 and 2) and the Power Switch (S1: pins 3 and 2/1).

The switch connection, however, is shown as *Multi Passives* (S1.3-S1.2, S1.3-S1.1) between NetD1_2 and 5V. To be completely accurate in terms of the current path, this can be changed to include only S1.3 and S1.2 between those nets (as indicated in the schematic). To modify the S1 pin settings, click its representative object box (designated as 'Multi Passives') and use the dialog to deselect the pins 3 to 1 option for S1.

When the change has been completed, the S1 object will then indicate a single pin-to-pin setting (S1.3 to S1.2) – in place of 'Multi Passives'. Note that the resistance represented by the passive components (here, F1 and S1) defaults to 0.001Ω but can be altered in their parameter dialogs.
The PWR_IN to 5V example simulation demonstrates the ability to use a different net at the source and loads, where the path between goes through passive components. These components can be modeled as a resistor only, whereas paths through active components need to have their input and output paths modeled separately. While the path from the source and load nets is automatically derived, that path may be modified to suit if necessary - see below.

The example's simulation results show that the voltage drop on the ground plane (GND), due to 5V current delivery, is only a maximum of 11µV, compared to 1.37mV for VCCINT and 5.3mV for VCCO. This is due to the large amount of ground shape between the source and the major loads, U3 and U4.

Source to Load path

In circumstances where a number of DC paths exist between the nominated Source and Load nets in a design, the PDN Analyzer may select an undesired Source to Load path – one that is not the primary, high-current flow path you had in mind.

The path that the Analyzer automatically selects is dependent on the circuit’s net topography, the presence of formally labeled nets and other factors. The process does not distinguish between connecting pins on active devices for example, or make any predictions that indicate the highest current path.

To allow the source to load path to be reconfigured to the correct set of nets, the PDN Analyzer interface allows individual nets to be removed from the path, therefore forcing the analyzer to adopt one of the alternative net paths. In practice, the undesired nets are simply deleted from the interface’s graphic representation of the source to load path.

By way of example, consider a simple power circuit that has three or four DC paths between the Source net (VCC) and the Load net (VSS).
When setting up a simulation in the PDN Analyzer, with the Source Power Net nominated as VCC and Load net as VSS, the analyzer may adopt one of three main paths between the desired nets. One is clearly the desired path – that directly through the regulator U1 – which is nominated as path C below.

In this example case however, the PDN Analyzer has automatically selected path A for the simulation, which passes through the nets associated with D2 and Q1. The PDN analyzer U1 will show those nets in the graphical representation of the source to load path.
The PDN Analyzer has automatically adopted path A as the source to load path, as shown by the nets included in the Analyzer’s GUI.

Here, the specific nets are:

- **NetD2_1** - junction of R6 and D2
- **NetD2_2** - junction of D2 and Q1
- **NetQ1_2** - junction of Q1 and R7

To correct the current path to the desired source to load path (C), begin by deleting any of the unwanted nets – as it happens, *none* of the included net are wanted in the path.

Removing a net from the path causes the Analyzer to adopt an alternative source to load path, in this case, it has moved to path By (see diagram above), which includes the undesired net; NetC3_1.

This includes nets:

- **NetC2_1** - junction of R1 and C2 (this is a desired net, as also included in path C)
- **NetC3_1** - junction of C3 and the GND pin of U1.
At this point it’s clear that one of the remaining nets (NetC3_1, in path Bx/By) should not be included. When this is deleted, the source to load path resolves to include just the desired net; NetC2_1.

The path is therefore as represented by path C in the above path diagram, and correctly includes just R1, NetC3_1 and U1.

![Path Diagram](image)

With erroneous nets removed, the Analyzer falls back to the desired simulation path; C.

## Metal Conductivity

When the PDN Analyzer panel’s Metal Conductivity link is clicked, the subsequent Metal Conductivity dialog provides details and settings for the conductivity value (inverse of resistivity; \(1/R\)) of the metal used in a design.

![Conductivity Settings](image)

The default metal used for simulations is **Pure Copper**, which is typically assumed to have a conductivity of 5.88e7S/m at 25°C, and a conductivity thermal coefficient of 0.4%/°C. This positive temperature coefficient means that raising the dialog’s **Temp. Compensation** setting from 25°C to 125°C (100°C delta) will lower the simulation conductivity by 40%, to 3.53e7S/m, for instance.

The alternative **PCB Copper** setting reflects conductivity values reported in industry literature as more representative of the metal found in PCB electro-deposited (ED) copper, which is measured to be 4.7e7S/m at 25°C, with a thermal coefficient of 0.4%/°C. Select the **Custom** option to enter a specific Conductivity or Resistivity value for a PI simulation.
The base conductivity (or resistivity), temperature coefficient, and/or temperature can be modified in the dialog to reflect a design’s metal properties. The Sim Conductivity figure represents the final conductivity value after taking into account all parameters.

**Via Wall Thickness**

Select the PDN Analyzer panel's Via Wall Thickness link to specify the weight of the Via wall metal for all Vias in the design simulation analysis.

The Via wall material thickness has a default value of 18µm (0.7mm) and a minimum simulation thickness of 1µm – if the Wall Thickness is set to less than that figure, a setting of 1µm is used. The setting can noticeably affect the power network DC losses due to the inherent resistance a thin-walled (-plated) Via represents. When of sufficient size/weight however, a Via will not impede a design's DC performance, and will show the same current density as the power traces it connects – and no significant voltage loss between its connection points. A DC analysis example of loss through Vias is shown above.

In terms of the simulation, the Via size and wall thickness effectively defines the amount of conductive material represented by the Via, and therefore its resistance/conductivity. The simulation assumes that the Via diameter represents the finished hole size, and the via wall thickness then increases the Via diameter. Therefore: Finished Hole Diameter + (2 x Wall_Thickness) = Drill Diameter.

**Result panel features**

Along with settings for the how the simulation board shapes are rendered in the Altium Designer’s PCB editor (Voltage/Current, Net and Layer), the PDN Analyzer Result panel window offers other settings and controls to manage the simulation results.
Most obviously, the panel’s **Display filter** section allows the span of visual results scale to be manually (rather than automatically) defined.

- To set a specific Voltage or Current Density range, select the **Manual** mode in the **Scale option** section. When new Min/Max values and have been entered and the **Update** button clicked, the PCB editor’s graphical scale settings, and in response the color gradient of the display, will change accordingly.

- Simulation Current Density results are displayed using the A/m² (amps per square meter) units by default. Select an alternative unit from the **Current density** drop down menu.

The panel’s **Results** section includes range of buttons for working with simulation data. These include:

- **Probe value**: This button activates a simulation data readout mode in the PCB Editor. When selected, the editor’s cursor will change to probe mode (purple colored 3D cursor or a 2D crosshair), where the underlying simulation data is reported to Altium Designer’s **Heads Up Display**. Simply click within a board shape to see a Voltage or Current Density readout for that specific location.

- **Clear**: Click to remove the simulation rendering in the PCB editor display – click to restore.
Click to change the display back to its last used conventional view (for example, Altium Standard 2D). The PI-DC simulation results will remain displayed as an overlay in the PCB editor, but can be cleared with the Clear button.

In some cases, such as when editing a board for a better PI result, it may be useful to retain the simulation rendering. To restore a cleared simulation display rendering, click the button.

To go back to the PDN Analyzer simulation results only, reselect one of the PCB editor's analyzer view modes (2D or 3D) and click Update, or simply re-run the simulation.

Select the rendered display type in Altium Designer's PCB Editor. The PDN Analyzer results will be rendered in 2D or 3D format, which is equivalent to selecting the Altium 2D PDN Analyzer or Altium 3D PDN Analyzer view options directly in the PCB Editor.

Opens a file browser view of the current PCB project's PDN Analyzer output directory. This contains the current simulation data, including a \Results subdirectory that contains the *.json and *.csv results files.

Loads a JSON formatted (attribute-value pairs) data file. For example, the analyzer's fields.json results file (located in the output \Results subdirectory) contains the Voltage/Current data results for all simulated Layers and Nets. Loading such a file will define the simulation data for the shapes in the current board layout.

Loads a conventional (semicolon delimited) CSV tabular data file. The analyzer's volt_curr.csv file in the output \Results subdirectory contains the parameter and voltage drop information for the current simulation.

Current Limitations

The PDN Analyzer extension's capabilities will be expanded over time to include the features and interface required to make the tool as effective as possible yet easy to use. There are currently some limitations in the depth of the analysis that can be performed, however these will be progressively reduced as the tool is developed.

Some of current feature limitations are:

- **Integrated schematic/PCB editing.** Net names and components cannot be directly entered from the schematic or PCB window.

- **Multiple sources.** Only allow a single, positive voltage source is allowed at present, rather than multiple sources and/or negative voltage sources (or negative current sink loads).

- **Source to load ground path.** Only a single ground net path is available between the source and load (unlike the multiple net path capability for power nets).

- **Spaces in component names.** Currently, the simulation will fail if the PCB design includes any components with space characters in the Designator. This will be resolved in the next release.

To troubleshoot and locate such an issue, check the design.dar.log file found in the project's \PDNAnalyzer_Output\Results\tmp directory. This will show a Syntax warning or error message that indicates a line number in the components file generated by the
To check that reference in the components file, it needs to opened/extracted from the tar archive file [project_name].tgz located in the \PDNAnalyzer_Output directory. This can be done using a compatible archive management tool, such as 7-Zip or similar.

Use the tool to navigate to and view the components file from the archive path \odb\steps\pcb\layers\comp_+_top (or comp_+_bot, as determined by the Syntax error). Refer to the line number indicated by warning/error in the design.dar.log file (above) to find the component name that is causing the issue. In the example shown here, the design's Voltage Regulator component (line 8) has a Designator that includes a space: U 1. This can be corrected in the PCB design to resolve the error.
Note that the above general list is likely to change or reduce during the course of development, and may not necessarily be up to date.

Source URL: https://www.altium.com/documentation/display/ADSF/((PDN+Analyzer+Example+Guide))_AD