The Situs Topological Router brings a new approach to the autorouting challenge. It uses advanced topological mapping to first define the routing path, then calls on a variety of proven routing algorithms to convert this ‘human-like’ path to a high-quality route. As an integral part of the PCB editor, it follows the PCB electrical and routing rule definitions.

While Situs is straightforward to set up and run, there are certain points you should be aware of to produce optimal routing of your board.

**Board setup**

**Component placement**

Ultimately, the component placement has the most significant impact on routing performance. Protel DXP includes a number of tools, such as dynamically optimized connection lines, that allow you to fine tune component placement. The optimal component placement is when the connection lines are as short and least ‘tangled’ as possible.

Other good design practices include placing components so their pads are on a regular grid (to maximize the amount of free space between the pads for routing), placing similar sized surface mount components exactly opposite each other on double sided boards, and consulting device manufacturers datasheets for decoupling placement guidelines. This is not a complete list of placement considerations, simply a few suggestions.

**Keepouts**

The router requires a closed boundary, made up of tracks and arcs on the keepout layer. Typically, this boundary is in from the edge of the board, a distance that satisfies any mechanical or electrical clearance requirements that the design may have. The router will also obey keepout layer definitions within this outer boundary, as well as layer-specific keepouts.

**Polygons**

Polygons, or copper pours, are constructed from tracks and arcs. A medium to large polygon includes a large number of these tracks and arcs. While the router can route a board that includes polygons, the sheer number of objects they introduce increases the complexity of the routing process.
Typically you should only place polygons prior to routing if they are required, for example, they are being used to construct unusually shaped pre-routing, perhaps the incoming mains routing or a critical ground region. Otherwise it is preferable that polygons be added to the design once routing is complete.

Is it routable?

An autorouter is a human attempt to understand and model the routing process, then replicate that process automatically. If the board contains an area that can not be routed by hand, then it will not be autorouted either. If the router is continually failing on a component or a section of the board then you should attempt to route it interactively. It may be that there are placement or rule configuration issues that make it impossible to route at all.

Pre-routing

Pre-route critical nets and, if it is essential that they are not changed by the routing process, lock them by enabling the Lock all Pre-routes option in the Situs Routing Strategies. Avoid unnecessary locking though; a large number of locked objects can make the routing problem much more difficult.

Configuring the Design Rules

Make sure the routing design rules are appropriate to the board technology you are using. Poorly targeted or inappropriate design rules can lead to very poor autorouting performance. Note that the router obeys all Electrical and Routing design rules, except the Routing Corners rule.

Basics

The DXP rules system is hierarchical. The idea is that you start with a default rule for all objects, then add additional rules to selectively target other objects which have different requirements. For example, you should have a default rule for the routing width which covers the most common routing width used on the board, then add subsequent rules to selectively target other nets, classes of nets and so on.

The most important rules are the Width and Clearance rules. These routing technology settings define how tightly the routing can be 'packed'. Selecting these is a balancing process – the wider the tracks and bigger the clearance, the easier it is to fabricate the board; versus the narrower the tracks and clearances, the easier it is to route the board. It is advisable to consult your fabricator to establish their ‘price points’ for routing widths and clearances, those values which if you go below will result in lower fabrication yields and higher priced PCBs. As well as satisfying the electrical requirements of the design, the routing technology should also be chosen to suite the component technology, to allow each pin to be routed to.

The third rule that is part of the routing technology is the Routing Via Style. It should also be selected to suit the track and clearances being used, while considering the fabrication costs of the chosen hole size and annular ring.
You should also avoid excessive or unnecessary rules – the more rules, the more processing time, the slower the routing. Rules can be disabled if not required for autorouting.

**Routing Width**

Ensure there is a Routing Width rule with a Query of All (a default rule), and that the Preferred setting is appropriate for the most common routing width you require. Make sure that this width, in combination with the appropriate clearance rule, allows all pads to be routed to. Configure additional routing width rules for nets that require wider or narrower routing. If there are fine pitch components that have pins on nets with wider routing widths – for example, power nets – test route out from a power pin and also route out the pin on either side to ensure that it is physically possible to route these pins.

**Clearance Constraint**

Check for special clearance requirements, such as fine pitch components whose pads are closer than the standard board clearances. These can be catered for using a suitably scoped and prioritized design rule, as shown in the image. Note that while you can define a rule to target a footprint, it will not target the routing that connects to that footprint. As mentioned in the Routing Width topic, test route to ensure that the component pins are routable.

**Routing Via Style**

Ensure there is a Routing Via Style rule with a Query of All and that the preferred setting is appropriate. Include higher priority rules for those nets that need a different via style than the default rule.

DXP supports blind and buried vias, when these will be used is determined by the drill pair definitions set up in the Layer Stack Manager. Like interactive routing, when the autorouter switches between two layers it checks the current drill pair definitions – if these layers are defined as a pair then the via that is placed will have these layers as its start and end layers. It is important to understand the restrictions to using blind/buried vias; they should only be used in consultation with your fabricator. As well as the restrictions imposed by the fabrication stackup technology, there are also reliability and testing accessibility considerations. Some designers consider it better to add more routing layers than to use blind/buried vias.

**Routing Layers**

Choose appropriate layer directions to suit the flow of the connection lines. Situs uses topological mapping to define routing paths, so it is not constrained to route horizontally and vertically. Typically it is best to have outer layers as horizontal and vertical. If, however, you have a multi-layer board with a large number of connections at a ‘2 O’Clock’ angle, then set one or more internal layers to have this as the preferred routing direction. The Layer Patterns pass in particular makes use of this information, and
choosing the right direction can make a significant difference to routing performance in terms of both
time and quality. Note that when you use angled layers you do not need to have a partner layer running
at 90 degrees to this layer, since the router will typically route horizontally or vertically if it needs to
avoid an obstacle on an angled layer.

Avoid using the Any direction – the layer that is chosen to route a connection on is based on how
closely the connection is aligned with the layer direction, so this layer becomes the layer of last resort.
The Any direction is typically only used on single-sided boards.

Routing Priority
Use the Routing Priority rules to set a higher priority on difficult nets, or those that you want to have the
cleanest routing.

SMD Fanout Control
The Query system includes keywords that specifically target the different surface mount component
packages including IsLCC (Leadless Chip Carrier), IsSOIC (Small Outline IC), IsBGA (Ball Grid Array)
and IsSMSIP (Surface Mount Single In-line Package). Default rules are automatically created for the
most common packages and since fanout passes are run early in the autorouting process, there is little
penalty in keeping rules that do not apply to any components. You should have at least one SMD
fanout control design rule if there are surface mount components on the board – a suitable query for a
single rule targeting all surface mount components would be IsSMTComponent. For information on
how each query keyword identifies a component package, open the Query Helper, type in the required
keyword and press F1.

The fanout rules include settings that control if the pads are to be fanned in or out, or a mixture of both.
To help become familiar with the behavior of the Fanout Control rule attributes, the Autoroute »
Fanout » Component command can be run on any surface mount component that has no nets
assigned to it. As well as using this to check how well a component fans out with the current routing
technology defined in the board, you can also use it to fan out a component that you want to keep in a
library as a pre-fanned out footprint. Once it is fanned out in the PCB workspace, copy and paste the
component and the fanout tracks and vias into a library.

Rule Priorities
The precedence, or priority, of the rules is defined by the designer. The rule priority is used to
determine which rule to apply when an object is covered by more than one rule,. If the priority is not
set correctly, you may find that a rule is not being applied at all.

For example, if the rule with a query of InNet('VCC') has a lower priority than the rule with a query of
All, then the All rule will be applied to the VCC net. Use the Priorities button in the PCB Rules and
Constraints Editor dialog to correct this. Note that priority is not important when two rule scopes do
not overlap (do not target the same objects). For example, it makes no difference which of these two
rule scopes has a higher priority – InNet('VCC') or InNet('GND').

The Golden Rule
Perhaps the most important step is to perform a design rule check (DRC) prior to starting the
autorouter. It is essential that any routing-related rule violations are resolved before starting the
autorouter. Not only can violations prevent routing at the location of the violation, they can also greatly slow the router as it continually attempts to route an unroutable area.

Always check the **Warnings** tab in the **Situs Routing Strategies** dialog before starting the autorouter.

## Running the router

Don't be afraid to experiment. If the results are not acceptable, do something to change the router’s approach. Add intermediate cleanup and straighten passes, make more room around dense areas or change the layer directions. As you experiment with the router – creating your own strategies to control the order of passes, changing the number of vias with the Via control, changing the routing layer directions, and so on – keep notes of the combinations that you have tried. That way you will be able to identify and reuse which configurations work best with your designs.

Run fanout passes on their own first and assess the quality. You may need to manually fanout any problem areas.

## Summary of the Routing Passes and Routing Strategies

The following routing passes are available. The passes can be used in any order, as a guide examine an existing strategy to see the order of passes.

### Memory

This is a connection level routing pass. It checks for two pins on different components on the same layer that share X or Y coordinates.

### Fanout

This is a component level pass, based on the fanout settings defined by the Fanout Control. It checks for patterns in pads, considers clearance, routing width and via style, then selects a suitable fan out arrangement (single row, staggered, etc) to meet the requirements defined in the design rule.

### Layer Patterns

This is a connection level routing pass. It only routes connections that match a layer direction (within a tolerance). It is costed to hug or follow existing routing to maximize free space.

### Main

This is a connection level routing pass. It uses the topological map to find a routing path, then uses the push and shove router to convert the proposed path to actual routing.

### Completion

This is a connection level routing pass. It is essentially the same as the Main pass, costed differently to resolve conflicts and complete difficult connections. Examples of costing differences include vias being cheaper and wrong-way routes being dearer.

### Straighten

This is a connection level routing pass that attempts to reduce the number of corners. It does this by walking along the route to a corner, then from that corner performs a (horizontal/vertical/45up/45down) probe searching for another routed point on the net. If one is found, it then checks to see if this new path reduces the routed length.
**Situs Autorouting Essentials**

**Hug**
This is a connection level routing pass that reroutes each connection, following existing routing with the minimum clearance possible. The hug pass is used to maximize free routing space. Note that this pass is very slow.

**Spread**
This is a connection level routing pass that reroutes each connection, attempting to spread the routing to use free space and equally space routing when it passes between fixed objects (such as component pads). Note that this pass is very slow.

**Clean Pad Entries**
This is a connection level routing pass. It reroutes out from each pad centre along the longest axis of the pad.

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**Revision History**

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<tr>
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