ALTUMLIVE 2018:
MIGRATING TO ALTUUM DESIGNER

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Thanks to Dave Cousineau for some original material.
Why Migrate?

The answers will determine how much time and effort will go into the exercise.
Know These 3+ Things

Establishing These up-front will profoundly affect the level of effort required.

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**Above all** – Understand the Altium Designer Unified Component Model
It is like no other EDA tool:

The Unified Component Model makes it possible to easily synchronize, back-annotate, and edit across PCB and Schematic, but the link needs to be re-established on Imported Data. Then you can edit, modify, and create libraries from the imported content.

Above all – Understand the Altium Designer Unified Component Model
Agenda

1. Typical Data Migration Process
2. OrCAD + Allegro To Altium Designer
3. OrCAD + PADS (or just PADS) to Altium Designer
4. Examples / Live Demo
5. Conclusions / Q & A
Optional Extras:
- ASCII is needed for only some importable formats (i.e., PADS)
- Libraries can be imported separately from CAD documents
- Unified Libraries can be created from imported SCH+PCB documents
- 3D Models can be added afterwards using library update or model manager
Agenda

1. Typical Data Migration Process
2. **OrCAD + Allegro To Altium Designer**
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Cadence Migration

• Translation Process
  • Source files
  • Import Wizard
• Post Processing
  • Project synchronization
  • File clean up
• Sample Translation
• OrCAD .DSN files directly supported
• Allegro requires an ASCII version of the .BRD
  • .ALG format
  • Created using “extracta.exe” tool (Cadence)
• Altium importer can run “extracta” if on the same computer
  • Point importer to .BRD files
• Otherwise, create .ALG file manually
  • Allegro2Altium.bat in <Altium install dir>\System
  • Copy this and all referenced “Allegro*.txt” to the Cadence computer
• Up to version 16.x currently supported
Source File Incompatibilities & Changes

• OrCAD
  • Net Groups imported as Sheet Symbols
    • Manually convert to Signal Harnesses
    • Copy Sheet Entries and use Smart Paste as “Harness Connector”

• Allegro
  • In-footprint component keepouts not supported
    • Converted as copper
    • Manually remove
  • In-footprint vias lose net connectivity
    • Use Design → Netlist → Update Free Primitives From Component Pads...
  • Slots imported as round holes
    • Manually adjust in Altium
• In Altium Designer, run File → Import Wizard
• Select *OrCAD Designs and Libraries files*
• Use the **Importing OrCAD Designs** screen for schematics (.DSN)
  • Multiple designs can be translated simultaneously
• Use the **Importing OrCAD Libraries** screen for libraries (.OLB)
  • Library translation is not necessary for design translation since parts are cached locally within the schematics
  • Multiple libraries can be translated simultaneously

• Default options are generally OK
Import Wizard: Allegro

• In Altium Designer, run File → Import Wizard
• Select Allegro Design files
  • .BRD files if Cadence PCB tools are on the same system
  • .ALG files produced elsewhere
• On Default PCB Specific Options screen, disable “Import Auto-Generated Copper Pour Cutouts”

• Current PCB Layer Mappings screen to:
  • Change target layers
  • Skip import of layers (“No Layer” setting)
Project Synchronization

- Schematics and PCB translated independently into different folders
- Move or copy translated PCB file (.PcbDoc) to schematic project folder
- Add .PcbDoc to schematic Project
- Component UIDs will be synced during ECO
File Cleanup

• Helpful Altium Designer tools for efficient cleanup
  • Navigator panel
  • Find Similar Objects
  • Properties panel
  • Pre- and Post-selection filters
  • PCB panel
  • Single Layer Mode (Shift + S)
Schematic File Cleanup

- Tools \(\rightarrow\) Convert \(\rightarrow\) Reset Component Unique IDs
  - Reset Duplicates
  - All schematic documents in current project
- Compile Project can help uncover connectivity problems
  - Set Connection Matrix (Project \(\rightarrow\) Project Options) to “All Off”
  - Error Reporting, “Nets with no driving source” to “No Report”
  - Avoids “noise” of non-critical warnings
- Nets with multiple names
  - Conflicting Off-Sheet Connector, Power Port, Net Label names
- Duplicate Net Names (Element or Bus Slice)
  - Busses without Net Labels
  - Duplicated names on Net Labels, Off-Sheet Connectors
Schematic File Cleanup

• ECO to PCB to locate any issues not found in schematic
  • Choose “Automatically Create Component Links” if prompted
• Focus on Net-based modifications
  • Remove or Add Pins from Nets
  • Remove or Add Nets
  • Change Net Names
• Only *Change Net Names* modifications should remain
  • Those should only be changing system-assigned net names
  • E.g., N21757673 -> NetC19_1
• Any other net changes indicate connectivity problems in the schematic
  • E.g., AGND -> LCD_DATA0
• Component, Class, and Room modifications will likely remain for now
PCB File Cleanup

- Recreate board outline (if necessary)
- Remove data from unnecessary mechanical layers
  - Use Single Layer Mode to isolate
  - “Select All On Layer” (S, Y) then <Delete>
  - Un-selectable data most likely embedded in footprint
- Remove extraneous data from footprints
  - Set selection filter to “Components” and select all
  - In Properties panel, unlock Primitives and Strings
  - Reset selection filter to “All Objects”
  - CTRL+Select unwanted data per layer and <Delete>
    - Take note of unwanted layer names for future imports
  - Reselect all components and re-lock Primitives and Strings
  - Save, close, and reopen .PcbDoc
- Remove Rooms
  - Only if used as Component Keepouts and
  - Only if placement will not change
PCB File Cleanup

• Change Type for mechanical components
  • E.g., fiducials
  • Project → Component Links to see list of “unmatched” components
  • Change Type from “Standard” to “Mechanical” in Properties

• Design Rules and Net Classes
  • Allegro design rules and net classes not imported
  • Recreate in Altium

• Polygon outlines may need to be edited or redrawn
  • Poured outlines transferred
  • Potentially many smaller polygon shapes to be removed or recreated

• Set Polygon Pour Order
  • Tools → Polygon Pours → Polygon Manager, Auto Generate in Pour Order section
  • Repour All afterwards
- Examine Keepouts
- Examine multi-layer padstacks
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1. Typical Data Migration Process
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PADS Logic & Layout Migration

- Translation Process
  - Source files
  - Import Wizard
- Post Processing
  - Project synchronization
  - File clean up
- Sample Translation
• PADS Logic & PADS Layout translations both require ASCII file exports

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<th>Source Files</th>
<th>Extension</th>
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<tr>
<td>PADS Logic Schematics</td>
<td>.TXT</td>
</tr>
<tr>
<td>PADS Layout PCBs</td>
<td>.ASC</td>
</tr>
<tr>
<td>PADS Decal (footprint) Libraries</td>
<td>.D</td>
</tr>
</tbody>
</table>

• .TXT and .ASC files created from PADS using File → Export...
  • Logic V9.0 or earlier
  • Layout V9.5 or earlier

• .P, .C, and .D files created from the PADS Library Manager
  • File → Library...
  • Set the Filter to the desired library section (e.g., “Decals” for .D)
  • Select the items to be exported (select first item in the list, then Shift + select the last to export the whole library section)
  • Click the Export... button
  • Repeat for each library section
Source File Incompatibilities & Changes

• PADS Logic
  • Individual pin connectors not supported
    • Change to “block”-style connectors in PADS, or
    • Replace in Altium Designer post-translation

• PADS Layout
  • Physical Design Reuse blocks must be broken apart
In Altium Designer, run File ➔ Import Wizard

Select PADS ASCII Design and Library Files

Use the Importing PADS Designs screen for schematics and PCBs
- Multiple files or both types can be translated simultaneously
- Use the pull-down to change file types

Use the Importing PADS Libraries screen for libraries
- Library translation is not necessary for design translation since parts are cached locally within the schematics and PCBs
- .C and .P files must be translated simultaneously to create schematic libraries
- Multiple .C/.P and .D files can be translated simultaneously
- PADS Logic schematic Import Wizard default options are acceptable
- Keeping “Do not translate hidden net names” enabled is recommended for schematic cleanliness
- Altium system-assigned net names can be sync’ed to PCB via ECO
• PADS Layout PCB design Import Wizard default options are acceptable
  • Ensure “Generate Teardrops” is disabled
• “Edit Mapping” button to remap target mechanical layers or adjust positive/negative plane layers
  • PADS CAM Planes → Altium Plane layers (negative)
  • PADS Split/Mixed Planes → Altium Plane layers (negative) if no routing
  • PADS Split/Mixed Planes → Altium Signal layers (positive) if routing exists
Project Synchronization

- Schematics and PCB translated independently into different folders
- Move or copy translated PCB file (.PcbDoc) to schematic project folder
- Add .PcbDoc to schematic Project
- In PCB editor, use Project → Component Links to synchronize UIDs (“unique IDs”)
File Cleanup

• Helpful Altium Designer tools for efficient cleanup
  • Navigator panel
  • Find Similar Objects
  • Properties panel
  • Pre- and Post-selection filters
  • PCB panel
  • Single Layer Mode (Shift + S)
Schematic File Cleanup

• Look for net labels at wire intersections

• Add Ports to busses that cross multiple sheets

• Delete all manual junctions
  • Use *Find Similar Objects* to select all across design
  • Delete sheet-by-sheet

• Visually scan schematics for out-of-place or overlapping objects
Schematic File Cleanup

• Compile Project can help uncover connectivity problems
  • Set Connection Matrix (Project → Project Options) to “All Off”
  • Avoids “noise” of non-critical warnings

• Nets with only one pin
  • Incorrect sheet to sheet connectivity

• Duplicate net names (bus slice or element)
  • Missing bus Net Label and/or Port

• Nets with multiple names
  • Misplaced net labels
  • Net labels at wire intersections

• Use “Allow Ports to Name Nets” setting in Project Options and remove extraneous Net Labels
Schematic File Cleanup

• ECO to PCB to locate any issues not found visually
• Focus on Net-based modifications
  • Remove or Add Pins from Nets
  • Remove or Add Nets
  • Change Net Names
• Only *Change Net Names* modifications should remain
  • Those should only be changing system-assigned net names
  • E.g., $$$490 -> NetR149_1
• Any other net changes indicate connectivity problems in the schematic
  • E.g., AGND -> LCD_DATA0
• Component, Class, and Room modifications will likely remain for now
PCB File Cleanup

• Change *Type* for mechanical or other non-“ECO registered” components
  • E.g., fiducials or mounting holes
  • Standard → Mechanical

• Review Design Rules
  • “Polygon Connect Style” rules
  • Min/Max Routing Widths and Via sizes
  • Remove any unused rules (High Speed, Same Net, etc.)
  • Add “IsKeepout” clearance rule set to 0

• Set Polygon Pour Order
  • Tools → Polygon Pours → Polygon Manager, **Auto Generate** in Pour Order section
  • Repour All afterwards

• Disable non-essential Design Rules for initial batch DRC checking
  • Tools → Design Rule Check, Rules to Check
  • E.g., Manufacturing, Placement, High Speed
  • Run *Design Rule Check*...
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Cypress CY8CKIT-059
Altera Cyclone-III Starter Kit