ALTUMLIVE 2018:
ALTUIM MORALITY GUIDE:
A FRAMEWORK TO WORK EFFICIENTLY
GET THINGS RIGHT AND HAVE FUN

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San Diego
Juul Labs, Inc. 9/26/2018
Engineer
Legal vs. Moral

What you CAN do

What you SHOULD do
Background
Before Altium...
File Naming Example

[#][SHEET NAME][project-subproject][purpose][pcb#].schdoc

06_POWER_SUPPLY_Project1-mainBoard_830-00081.schdoc
Folder Structure (Altium)

• Documents > Altium
  • > 3D
    • > Connectors
    • > Diodes
    • > Electromechanical
    • > ICs
    • > Misc
    • > Modules
    • > Mounting HW
    • > Passives
  • > Libraries
    • > Capacitors
    • > Connectors
    • > Diodes
    • > Electromechanical
    • > ICs
    • > Inductors
    • > Misc
    • > Modules
    • > Resistors
    • > Transistors

• Manufacturing
  • > FAB notes generator (excel)
  • > Manufacturing reference stuff
  • > DFM Guidelines

• Simulation
  • > SPICE models

• Templates
  • > BOM Templates
  • > SCH Templates
  • > PCB Tempaltes
  • > Output Job Files
Folder Structure (Projects)

- Documents > Hardware
  - > Project1
  - > Project2
  - > Project3
  - > ProjectN
  - Workspace1
  - Workspace2
  - Workspace3

- Project1
  - > Outputs
    - > PDF Documentation
    - > Binaries
    - > STEP 3D
  - > History
  - > Logs
  - > Other
  - > Datasheets
  - Source Files
Version Control

• Revision # should be in all Schematic Documents and PCB Files:

- Sample approach:
  - Major.Minor ie 12.3
  - Major incremented on release
  - Never have 2 boards that are fab’d with the same major number
  - Minor incremented on changes
  - Increment every commit if using GIT/SVN
  - Minor striped on release to fab: 1.1, 1.2, 1.n -> Release 1
  - Updates after released, increment major with minor: Release 1 -> 2.1, 2.n, Release 2
  - Pre-production revs are numeric
  - Production uses Alpha/Beta/EVT/DVT/PVT
Version Control
Altium Configuration
Navigation

Preferences

Highlight Methods
Choose here the methods used to highlight graphical objects during navigation. These options are used during navigation, cross-probing, and when exploring differences between documents or design sessions.

- Selecting
- Zooming
- Connective Graph
- Drumming
- Include Power Ports

Objects To Display
Choose here the objects to display in the Navigator Panel.

- Pins
- Net Labels
- Ports
- Sheet Entries
- Sheet Connectors
- Sheet Symbols
- Graphical Lines

Cross Select Mode
This mode gives the ability to select objects between the Schematic and PCB editors. When this mode is on, each selected object will be selected in the open documents of the other editor. For finding objects from a PCB in a closed schematic document, it is necessary to use the cross select tool.

- Cross Selection
- Dimming
- Zooming
- Reversion selected component in PCB Feedby: Ctrl+Shift+I
- No
- Components
- Net
- Focus document containing selection if visible

Design Insight
Define here which feature of Design Insight you would like to enable.

- Enable Document Insight
  - Document insight displays a preview of the documents from both the Projects panel and the Documents Bar. Hover over the document icon or enter location to view the preview. Click on the preview to open that document.

- Enable Project Insight
  - Project Insight provides a table of document previews for easy navigation. Hover over the Project icon in the Projects panel to gain insight into the documents in the project. Navigate to a document by clicking on it in the preview.

- Enable Connectivity Insight
  - Connectivity Insight shows the connectivity relationship of the set objects. The Insight will show preview of the sheet pages for sheet symbols, preview of the net connectivity across the whole project for electrical objects, and preview of the sub-parts for components. The preview will be organized according to the project hierarchy. Clicking on the file names in the document tree will open that document. Further customization is available in the options below.

- Enable Supply Chain Insight
  - Supply Chain Insight displays supply chain information from components that contain manufacturer part choices. Both pricing and availability can be examined. It is possible to add and remove manufacturer part choices by clicking on the Edit link.

- Enable Hyperlink Insight
  - Hyperlink Insight displays a link over hyperlinks and objects and annotations and parameters that have a URL or website as their last string. Use the View > Open external links in external browser preference to determine whether websites should be opened in DXP or externally.

Mouse Hover (Delay): 0s 4s

Connectivity Insight Options
- Insight Content to Show
  - Document Tree
  - Document Preview
  - Object Hints

Launch Style
- Document Tree
- Document Preview
- Object Hints
Design Insight (needs compile)  Connective Graph
Other configuration stuff…

- Data Management (not covered)
- Schematic
  - Compiler
  - Autofocus
  - Library Autozoom
  - Grids
  - Break Wire
  - Defaults
- PCB Editor
  - BI Color Overrides
  - DRC Violations Displays
  - True Type Fonts
  - Defaults
  - Reports
  - Layer Colors
  - Models
- Text Editors
- Scripting System
- CAM Editor
- Simulation
- Draftsman
- Multi-board schematic
- Multi-board Assemby
Mouse and Keyboard

• Mouse conf: Don’t change it!
• Memorize keyboard shortcuts
• SCH Favorites:
  • G (cycle thru standard grids)
  • P (place)
  • Tab (properties)
• PCB Favorites:
  • S,Y (select all on layer)
  • D, S, D (define PCB from selected objects)
  • Shift+space (cycle thru routing corner styles)
  • P (place), B (3D body)
  • Q (switch English/metric)
  • Tab (properties)
  • Shift+spacebar (corner style shift)
  • Shift+R (conflict resolution shift)
Containers (Projects, Workspaces) Guidelines
Workspaces
Schematic Capture Guidelines
Use Templates!
# Ducky Industries

**Board Name:** Ze Project Title  
**PCB Number:** 0000yyy-999  
**Assembly Number:** 0000xxx-555

## Table of Contents

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<th>Page Name</th>
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<td>Main Block and I2C Diagram</td>
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<td>Main Power</td>
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<td>TPM</td>
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</table>

## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Change Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5/04/2018</td>
<td>Initial Draft Design</td>
</tr>
<tr>
<td>5/18/2018</td>
<td>Release Draft</td>
</tr>
<tr>
<td>6/1/2018</td>
<td>Draft Ready for Review</td>
</tr>
<tr>
<td>6/12/2018</td>
<td>RTP, 1st Fab</td>
</tr>
</tbody>
</table>
Include a System and Power block diagram
USE STANDARD GRIDS!!!

USB CONNECTORS

USB ESD Diodes are more rugged than those for MMCX RF Connectors.

UART1 (Debug/Console)

3V3 TTL Signaling (USE FTDI 3V3 Cable)

UART3

3V3 TTL Signaling (USE FTDI 3V3 Cable)
Design notes/calculations

**Notes:**

1. Notes:
   - \( V_{in} = \frac{18\text{mV}}{\text{Vin} + 1} \times 0.6 \)
   - \( = \frac{0.00015}{0.5 + 1} \times 0.6 = 3.32V \)

**Note:**
SN74AVC41T234 has an Input-Disable Feature that allows Floating inputs. This is important because 1V_0 A/B can be shut down. No PU/PD resistors needed.
Clean up DRCs (markers)
5.5V (max) 6.0V ABSOLUTE MAX

Follow signal path
Use Multisheet designs
Avoid spiderwebs...
Display important parameters
Ensure Sync at all times!
USB ESD Diodes are more rugged than those for MMCX RF Connectors.
Design Variants

1. Click here

2. Click on the X to remove components interactively

First, select the newly created variant.
Hierarchical Design
Layer naming and purpose
Assembly layer
## Fabrication Layer

<table>
<thead>
<tr>
<th>Layer</th>
<th>Metal Type</th>
<th>Orientation</th>
<th>Thickness</th>
<th>Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>Copper</td>
<td>Horizontal</td>
<td>0.015 mm</td>
<td>N/A</td>
</tr>
<tr>
<td>Bottom</td>
<td>Copper</td>
<td>Vertical</td>
<td>0.015 mm</td>
<td>N/A</td>
</tr>
</tbody>
</table>

### CON MANUFACTURE IMPEDANCE TABLE

<table>
<thead>
<tr>
<th>Layer</th>
<th>Metal Type</th>
<th>Orientation</th>
<th>Impedance / Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>Copper</td>
<td>Horizontal</td>
<td>50 ± 10%</td>
</tr>
<tr>
<td>Bottom</td>
<td>Copper</td>
<td>Vertical</td>
<td>50 ± 10%</td>
</tr>
</tbody>
</table>
Outlines grids and origin
## Design Rule Verification Report

**Date:** 9/27/2018

**Time:** 3:44:31 AM

**Elapsed Time:** 00:00:39

**Warnings:** 0

**Rule Violations:** 0

### Summary

<table>
<thead>
<tr>
<th>Warnings</th>
<th>Count</th>
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</thead>
<tbody>
<tr>
<td>Total</td>
<td>0</td>
</tr>
</tbody>
</table>

### Rule Violations

<table>
<thead>
<tr>
<th>Violation Description</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clearance Constraint 5.0mil (A)(A)</td>
<td>0</td>
</tr>
<tr>
<td>Clearance Constraint 5.0mil (H) footprints [CM22] OR Has footprint [CM22] OR Has footprint [CM22] (L)</td>
<td>0</td>
</tr>
<tr>
<td>Clearance Constraint 10mil (I) (InfraDefPolygons) (TOP GND, POLY 1/2 track AND InNet[GC, ANT1] OR InNet[GC, ANT2])</td>
<td>0</td>
</tr>
<tr>
<td>Clearance Constraint 5.0mil (I) (InfraDefPolygons) (BOT GND, POLY 1/2 track AND InfNetClass[900HM, DIFF])</td>
<td>0</td>
</tr>
<tr>
<td>Clearance Constraint 5.0mil (I) (Track AND OthLayer/Top Layer) AND (InNet[TVB, A] OR InNet[TVB, B] OR InNet[TV1 SW] OR InNet[AG, ANT1] OR InNet[AG, ANT2])</td>
<td>0</td>
</tr>
<tr>
<td>Short Circuit Constraint (Allowed = No) (ALL)</td>
<td>0</td>
</tr>
<tr>
<td>Un-Routed Net Constraint (A)</td>
<td>0</td>
</tr>
<tr>
<td>Modified Polygon (Allow modified: Yes, Allow sheared: Yes)</td>
<td>0</td>
</tr>
<tr>
<td>Width Constraint (Min=5.4mil) (Max=10mil) (Preferred=5.5mil) (ALL)</td>
<td>0</td>
</tr>
<tr>
<td>Width Constraint (Min=3mil) (Max=10mil) (Preferred=3mil) (I) (OthLayer/Top Layer) AND (InNet[TVB, A] OR InNet[TVB, B] OR InNet[TV1 SW])</td>
<td>0</td>
</tr>
<tr>
<td>Width Constraint (Min=500ohms) (Max=500ohms) (Preferred=500ohms) (InfNetClass[RF, NET])</td>
<td>0</td>
</tr>
<tr>
<td>Width Constraint (Min=3mil) (Max=10mil) (Preferred=3mil) (InfNetClass[900HM, DIFF])</td>
<td>0</td>
</tr>
<tr>
<td>Width Constraint (Min=17.86mil) (Max=17.86mil) (Preferred=17.86mil) (InfNet[GC, ANT1] OR InNet[GC, ANT2])</td>
<td>0</td>
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<tr>
<td>Routing Via Min=0mil (Max=10mil) (Preferred=0mil) (MaxWidth=10mil) (MaxWidth=10mil) (Preferred=10mil) (ALL)</td>
<td>0</td>
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<tr>
<td>Differential Pairs Uncoupled Length using the Gap Constraints (Min=1mil) (Max=5mil) (Preferred=1mil) (Max=10mil) AND Width Constraints (Min=10mil) (Max=12mil) (Preferred=12mil) (InfNetClass[900HM, DIFF])</td>
<td>0</td>
</tr>
<tr>
<td>Power Plane Connect Rule (Direct Connect) [Expansion=20mil] (Conductor Width=10mil) (Avg Gap=10mil) (Diodes=4) (ALL)</td>
<td>0</td>
</tr>
</tbody>
</table>
Placement and Routing
Output Job Files
Output Job Guidelines (Relative Paths and Parametric names)
Library Management
Library Usage
The (10) Commandments…

• You shall always generate proper PDF Documentation with your Output Job Files.
• You shall always place components and routing on the chosen grid (5mil is great).
• You should split libraries functionally. Yes it applies to footprints too. Use level of granularity that makes sense for your organization.
• You shall not use polygon pours instead of planes unless strictly needed (impedances/flex/etc)
• You shall always terminate traces at center of pad.
• You shall use netnames and buses appropriately. No spiderwebs of wires.
• You shall only use Schematic Sheet Symbols for Hierarchical or multi-channel designs. Use something else for block diagrams.
• You shall split schematics into multiple sheets, use off-sheet connectors, ports and power ports.
• You shall ALWAYS review Gerbers and output files. This is part of the design process.
• You shall follow the layer naming convention for PCBs and never break it
• NEVER EVER EVER allow DRCs before releasing a design. Always make sure your DRCs are updated. Use often and use carefully. Applies to SCH and PCB BOTH.

• Make sure you keep SCH/PCB synchronized at ALL times. Do this after adding/changing anything important.

• Follow a strict process to manage libraries from creation to editing to validation. This applies to SCH/PCB/DBL/Other libraries. If you are lucky enough to have a librarian team/role, they should enforce the process.

• Never change default colors on system objects. Especially netnames. Goes without saying... don’t use those colors for anything else!

• Always use default grids on SCH capture! You can cycle through the standard grids by typing G shortcut

• Always use DETAILED 3D models for your footprints. It isn’t just cool and nice it is good practice.

• Always match SCH components to live components through the Supplier workspace panel. This ensures that your components are detailed and have all the needed information on their parameters list.