DETERMINE THE VALUE OF THE JTAG INTERFACE DURING SCHEMATICS STAGE

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Validating HW without firmware and without test pads

IEEE 1149.1

Standard since 1991 and still evolving

A.k.a. JTAG (Joint Test Action Group)
At the basis boundary-scan is about testing the presence of connections between components:

- At board level: connections between chips
- At module level: connections between boards
- At system level: connections between modules

Using (test) resources embedded in chips
Boundary-scan is also used for

- In-system device programming
  (cPLD’s, FPGA’s, Microcontrollers, Flash memories and many special devices)

- Software debugging

- Others: Fine-tuning circuits, reading built-in sensors (eg temp), etc.
Adding Boundary scan to a device

Boundary-Scan Register

- **TDI (Test Data In)**
- **TDO (Test Data Out)**
- **TMS (Test Mode Select)**
- **TCK (Test Clock)**
- **TRST (Test Reset)**

**TAP (Test Access Port) (JTAG)**

- **Instruction Register**
- **Core**
- **Bypass**

I/O connections to the device's inputs and outputs.
Testing interconnections

Testvector \( xx11111xx \)

Caused by an open underneath this pin

Mismatch!
Testing through connectors!

- DIOS
- Other board
Testing Memory connections

Need access to:
- Address bus
- Data bus
- Control signals

Examples:
- SRAM
- DRAM
- SDRAM
- DDR2
- DDR3
- DDR4
- …
Testing connections through combinatorial logic

Examples:
- And
- Or
- Nand
- ….
Testing connections through sequential logic

Examples:
- ADC / DAC
- I2C components
- Clock toggle test
- SPI components
- Calibration components
- RS232
- Ethernet chips
- Interactive applications
- ...
LVDS Interconnect test .6
LVDS Interconnect test .6
Using Debug & IP blocks for testing Peripherals

**uC’s:**
- ARM
- Analog Devices
- Freescale
- Infineon
- Microchip
- Texas Instruments
- Xscale
- NXP
- ST
- Samsung

**FPGA’s:**
- Altera
- Xilinx
- Actel
- Lattice
Programming NAND / NOR Flash
Programming uC’s

- Analog Devices
- Atmel
- Cypress
- Freescale
- Infineon
- Microchip
- Nordic
- NXP
- Philips
- Renesas
- ST
- Silicon Labs
- TI
- ....
Programming Logic

- JAM
- STAPL
- SVF
- Jedec
- IEEE 1532
- Actel
- Altera
- Lattice
- Xilinx
Testing and programming at system level
Summary Capabilities

- Interconnections between Bscan pins
- Testing through Connectors
- Resistors presence; Serial Pull-up / Pull down
- LVDS connections
- Emulative testing
- At speed memory interconnection test
- Using Embedded instruments
- ISP of Flash, uC, FPGA’s, cPLD’s

What can be used on your design?
DFT Definitions

1. Accessibility via:
   - Boundary Scan
   - Connector Pins
   - Test Points

2. Testability
   - Accessible, but testable? Drive and sense on a net?
   - Is it safe to drive a value on an accessible net?

3. Coverage
   - Which potential production failures (Pres., Val., Pol., Solder.) will be found by the total test strategy
DFT analysis during schematic stage

Schematics

Accessibility

Testability

Test Generation

Coverage

Layout

HW Engineer

(Bscan) Test Engineer

Layout Engineer
Check possibilities during schematic capture!

How?

- Test development house
- Use JTAGMaps, a free Altium extension
Only If schematic analysis shows that you have
  o a too low testability
  o a too slow programing process

If so, then add these to your schematics:
  • TP Digital <n> <level>
  • TP Analogue <n> <voltage>

..and recalculate the testability
I’m not using it for test because:

- Boundary scan devices are more expensive
- It adds tracks
- It adds more work during design
- Investment in tools
- It is all new to me, I don’t have time to learn
- I only do one complex design per year, learning curve
- Our EMS uses other test methods for electrical test

Why not think again because:

- FPGA’s, uC’s,... can NOT be purchased without it
- Only 5 to ~10, but minimizes number of Test Points
- Less Test Points placing, Quicker Prototype HW validation
- Some FOC Tools are on the market, Services, Temp. licenses
- Training on the job during your design process
- Out source analysis and Test pattern generation
- Flying Probe and ICT are more expensive & lower coverage
Summary: Benefits using Boundary Scan

- Testing HW without firmware
- Minimizes number of design cycles
- Minimizes number of Test Points
- Tests are already available during prototype stage
- High coverage of more complex designs
- Good failure localization
- One interface for testing and programming
- One test & ISP strategy for all product life cycles
- Simplifies tester configuration and fixture
Focus on:

✓ Cost, drives out quality
✓ Quality, drives out cost
Demo’s at our table in the expo area:

- Analysis of schematics with JTAG Technologies’ free extension for Altium called JTAGMaps
- Boundary scan Application development station: JTAGLive and ProVision
- Boundary scan stand alone production station

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Thank you for your attention!