ALTIUMLIVE
High-Speed Board Design Rules to Get Your PCB Designed Right the First Time

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My name is: Shalom Shlomi Zigdon

CEO of iTech iCollege – Board Design Academy
1981-2001 20 yrs as HW Engineer, VP Engineering, Startup CEO
2014-2018 Chairman of IEEE Symposium Signal Integrity & EMC
2017-2018 TAC [Technical Advice Committee] member of EDI CON, USA
2002-today Hi-Speed Consultant for SI/PI/EMC + PCB Layout
Lecturer and CEO at Board Design Academy for SIPI&EMC
1981 B.Sc. in Electronics, Technion, the Israel institute of technology.
1985 M.A in Project Management, University of Haifa, Israel
2002 C.I.D. at Silicon Valley IPC Designers Council

IPC - A committee-member of 3 IPC Standards:
IPC-2251 Hi-Speed Board Design for Signal Integrity
IPC-2221 PCB Design
IPC-2226 HDI- Hi Density PCBs Design.
10 Gifts in 40 Minutes to close the gap between Scheme and PCB

Outline

1. Know your Hidden Snakes in your Scheme
2. SI/PI/EMI main problems caused by PCB
3. The Return Current Path Disasters
4. Design your Copper well
5. Practical guidelines to the PCB Layout Design
Right the First Time?

The Beginning

1. In the beginning God created the heavens and the earth.
31 God saw all that he had made, and it was very good. And there was evening, and there was morning—the sixth day.

23 So the LORD God banished him from the Garden of Eden to work the ground from which he had been taken.

Paradise with the Snake is not a Paradise.
Seven days from now I will send rain on the earth for forty days and forty nights, and I will wipe from the face of the earth every living creature I have made.”

Even God did not create the world Right the First Time!!!
The Cure for Snakes

Be your Moses
Design your Copper Conductors and Power Plans
for Success of your PCB

a Copper Snake Designed by Moses
Your Mission:

To stay in the Paradise of your Schematic Design by............................

Eliminating or Decreasing the influences of the Snakes hidden in your PCB

During your Schematic Design, Not during the PCB Layout Process!!!
Is the Schema a Paradise?
Identify and Catch the Snakes

Set model = Chip model + Package model + PCB model

LSI Core Noise I/O SSN

EMI from Signal Layer

Packag

Signal Layer

Power Layer

LSI

PCB (4Layer)

EMI from Power Layer

PCB Noise
Snakes in the real PCB

• The return current path is The **hidden** parts of the **Signal Path**

• Materials: Dielectric Constant & Loss Tangent of Basic Dielectric
• Resistance & Inductance of Copper Conductors
• Parasitic Capacitance between Conductors and Planes
• Mutual Inductance >>>>>>> Crosstalk by Coupling
• Mutual Capacitance >>>>>>> Crosstalk by Coupling
• Switching Signals radiates Electromagnetic Fields
The Hidden Harmonics of the Switching Signal

[The AC of the DC]

the highest sine wave frequency component that might be in the signal

\[
BW[\text{GHz}] = \frac{0.35}{RT[\text{nsec}]} \quad \text{or} \quad RT[\text{nsec}] = \frac{0.35}{BW[\text{GHz}]}
\]
The Switching Signal

Most of signal integrity issues are caused by rise time effects. Signal integrity issues fall into four categories:

1. Radiated effects (e.g., EMI, crosstalk)
2. Inductance effects (e.g., ground bounce)
3. Reflection issues (related to transmission lines)
4. Resistance as a function of frequency (skin effect, dielectric losses)
The Switching Time

During Switching time \([t_R, t_F]\)

\[
\begin{align*}
\frac{dV}{dt} & \quad \text{Causes} \quad \text{Electric Field} \quad \text{Capacitance} \\
\frac{dI}{dt} & \quad \text{Causes} \quad \text{Magnetic Field} \quad \text{Inductance}
\end{align*}
\]

The Signal has the potential to be an Electromagnetic Field propagating between the Conductor and the Reference Planes
Electric Fields and Self Inductance during Switching Time [Rise Time or Fall Time]

Reduce Self Inductance of Conductors by minimizing length and/or by maximizing width

$L_{self} \sim \frac{\text{length}}{\ln w}$
High-Speed Signal AURA

The Electromagnetic Field Territory
James Clerk Maxwell

Maxwell’s Equations
1. Guass’s Law – The greater the charge, the greater the electric field
2. Guass’s Law for magnetism - Magnetic flux is zero through a closed surface
3. Faraday’s Law – An electric field is produced by a changing magnetic field
4. Ampere-Maxwell Law - A magnetic field is produced by a changing electric field (moving charge)
\[
\n\n\begin{align*}
(1) \quad \nabla \cdot E &= \frac{\rho}{\varepsilon_0} \\
(2) \quad \nabla \times E &= -\frac{\partial B}{\partial t} \\
(3) \quad \nabla \cdot B &= 0 \\
(4) \quad c^2 \nabla \times B &= \frac{\partial E}{\partial t} + \frac{j}{\varepsilon_0}
\end{align*}
\]

[0] An electric current \( j \) causes circulation of \( B \) \( (\nabla \times B) \)

[1] A changing magnetic field \( \frac{\partial B}{\partial t} \) causes circulation of \( E \) \( (\nabla \times E) \)

[2] A changing electric field \( \frac{\partial E}{\partial t} \) causes circulation of \( B \) \( (\nabla \times B) \)
The Fourier Transform

Signal on Time Domain is a sum of infinite Analog Waves on Frequency Domain.

\[ \hat{f}(\xi) = \int_{-\infty}^{\infty} f(x) e^{-2\pi i \xi x} \, dx \]

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Fourier composition of a sawtooth wave
Fourier composition of a square wave
PLACEMENT RULES

Analog Circuit [No Hidden Currents]
Follow the Schema For best Placement starting w Hi-Current

Voltage Adjust
Crosstalk internal Balanced Striplines

Layer Stackup: Design_xt_trace_separation.f.t
HyperLynx LiraSim v9.1

TOP
VCC
Inner1
Layer_01
Layer_02
Inner2
GND
BOTTOM

1 oz
0.5 oz
4 mils
1 oz
4 mils
1 oz
4 mils
1 oz
2 mils
1 oz
4 mils
1 oz
4 mils
1 oz
4 mils
1 oz
4 mils
0.5 oz
1 oz

Total thickness = 38.15 mils

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Fact: current flows in a loop
There must be a return current

Today, in Digital Design, any “Line” in Schema is actually a Loop in the PCB/System behaving as an “Unwanted Antenna”
Hi-Speed Return Current

For F>100 KHz, the Signal Returns through lowest Inductance (Loop Area) and highest Capacitance

The PCB layout sets the Return Current Path
Return current path
= Shortest possible connection

- DC: Less Resistance
- AC: Less Impedance
Hi-Speed Signal Conductor crossing split plane

Don’t Route
Digital Signal Conductor
Over Gap in the Plane underneath

$L \approx 5D \ln \left( \frac{D}{W} \right)$

$T_{\text{composite}} = \left[ \left( T_{10-90 \ L/R} \right)^2 + \left( T_{10-90 \ \text{signal}} \right)^2 \right]^{\frac{1}{2}}$

$T_{10-90 \ L/R} = 2.2 \frac{L}{2Z_0}$

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High Speed Digital Design: A Handbook of Black Magic
Hidden Currents in Scheme
No visible Power Supply pins
No Return Current Path
No Visible Loops

As a result, the R&D Engineer, fails to communicate essential information to the PCB Designer
Estimate the “Hidden Current” of the Hi-Speed Signals

The Six options:

Microstripe closed to GND Plane

Low-to-High Transition,
High -to- Low Transition

Microstripe closed to VCC Plane

Low-to-High Transition,
High -to- Low Transition

Stripline between Power Planes

Low-to-High Transition,
High -to- Low Transition
The hidden parts of the Signal Path
DIGITAL CIRCUIT CURRENT PATH
Trace Adjacent to a Ground Plane (Microstrip)

Low-to-High Transition

Current Source: Bypass/Decoupling Capacitor
Return Current Path: GND / Vss Plane
DIGITAL CIRCUIT CURRENT PATH
Trace Adjacent to a Ground Plane (Microstrip)

**High-to-Low Transition**

Current Source: Parasitic Capacitance
Return Current Path: GND / Vss Plane
DIGITAL CIRCUIT CURRENT PATH
Trace Adjacent to a Power Plane (Microstrip)
Low-to-High Transition

Current Source: Parasitic Capacitance
Return Current Path: Power/Vcc/Vdd Plane
DIGITAL CIRCUIT CURRENT PATH
Trace Adjacent to a Power Plane (Microstrip)

High -to- Low Transition

Current Source: **Bypass/Decoupling Capacitor**
Return Current Path: **Power/Vcc/Vdd Plane**

![Diagram of digital circuit current path with bypass/decoupling capacitor and return current path to power plane.](image-url)
DIGITAL CIRCUIT CURRENT PATH
Trace Between a Power & Ground Planes (Stripline)

Low-to-High Transition

Current Source: **Bypass/Decoupling Capacitor & Parasitic Capacitance**

Return Current Path: **Power/Vcc/Vdd Plane & GND / Vss Plane**
DIGITAL CIRCUIT CURRENT PATH
Trace Between a Power & Ground Planes (Stripline)
High-to-Low Transition

Current Source: Bypass/Decoupling Capacitor & Parasitic Capacitance
Return Current Path: Power/Vcc/Vdd Plane & GND / Vss Plane
Minimize the Loop Area IC-Capacitor
Power Conductors rules for EMC & SI

**Worst**  long & Thin Conductor
Higher Self-Inductance $>>$ EMI

**Better**  Short & Wide Conductor
Minimize Self-Inductance

**Preferred**  3 Vias act as 3 Inductors in Parallel result as $1/3$ Self Induction
The Real Capacitor

\[ z_c = x_L + x_c + R = j2\pi FL + 1/j2\pi FC + R \]

**frequency**
- Low
- Self-Resonance
- High

**impedance**
- Capacitive
- Resistive
- Inductive
Impedance of Various 100µF Capacitors

The Big V shape
Any loop Generates Radiation – “Antenna”

\[ E_{(V/m)} = 1.3 f_{(MHz)}^2 * A_{(cm^2)} * \frac{I_{(amps)}}{R_{(meters)}} \]

Minimize the dielectric thickness between Signal Layers and Power Planes

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Dont Rout the same Signal in the Cage
Add Stitching Via
Rout the **same Signal** closed to the **same Power Plane**

Returning signal current at this via pops between the top and bottom surfaces of the solid reference plane by passing through the clearance hole.
Faraday Cages
Do it the right way
Prevent Fringing Fields

20 H RULE

GND Plane

POWER Plane

POWER +

GND -
Start with the End

Choose the PCB Manufacturer before starting PCB Layout

• To get the best Layers Construction for:
• Impedance Control calculating with the real Dielectric Constant of the Laminates exist in storage
• Exact Dielectric Constant & Loss Tangent for each thickness of the Dielectric Core/Prepreg
• Using the minimum TH Via’s diameter to improve Power Integrity
• Copper Balance to eliminate disconnections pins-pads
• due to Bow & Twist Effect
Copper Balance
In case of non balance – fill the Signal Layers in GND Copper
### Thicknesses After Processing

#### Internal Layer Foil

<table>
<thead>
<tr>
<th>Copper Foil</th>
<th>Minimum</th>
<th>Minimum Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/8 oz</td>
<td>3.5 μm</td>
<td>0.000138 in</td>
</tr>
<tr>
<td>¼ oz</td>
<td>6.0 μm</td>
<td>0.000236 in</td>
</tr>
<tr>
<td>3/8 oz</td>
<td>8.0 μm</td>
<td>0.000315 in</td>
</tr>
<tr>
<td>½ oz</td>
<td>12.0 μm</td>
<td>0.000472 in</td>
</tr>
<tr>
<td>1 oz</td>
<td>25.0 μm</td>
<td>0.000984 in</td>
</tr>
<tr>
<td>2 oz</td>
<td>56.0 μm</td>
<td>0.002205 in</td>
</tr>
<tr>
<td>3 oz</td>
<td>91.0 μm</td>
<td>0.003583 in</td>
</tr>
<tr>
<td>4 oz</td>
<td>122.0 μm</td>
<td>0.004803 in</td>
</tr>
</tbody>
</table>

![PCB Cross Section](image)

### External Layer Foil Thickness After Plating

<table>
<thead>
<tr>
<th>Copper Foil</th>
<th>Minimum</th>
<th>Minimum Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/8 oz</td>
<td>20 μm</td>
<td>0.000787</td>
</tr>
<tr>
<td>¼ oz</td>
<td>20 μm</td>
<td>0.000787</td>
</tr>
<tr>
<td>3/8 oz</td>
<td>25 μm</td>
<td>0.000984</td>
</tr>
<tr>
<td>½ oz</td>
<td>33 μm</td>
<td>0.001299</td>
</tr>
<tr>
<td>1 oz</td>
<td>46 μm</td>
<td>0.001811</td>
</tr>
<tr>
<td>2 oz</td>
<td>76 μm</td>
<td>0.002992</td>
</tr>
<tr>
<td>3 oz</td>
<td>107 μm</td>
<td>0.004213</td>
</tr>
<tr>
<td>4 oz</td>
<td>137 μm</td>
<td>0.005394</td>
</tr>
</tbody>
</table>

![PCB Cross Section](image)
Fiber-glass Woven types

7628

2116

1080
Layers Construction

- Manufacturer recommendation PCB Layers Construction is a real Design
- Impedance calculation calculated with the real PCB Materials in storage
- Exact Dielectric Constant, Loss Tangent for each thickness of the Dielectric Cores/Prepreg
3D drawing of a microstrip transmission line  

Cross-section of a microstrip
The Finished Thickness influence the Impedance

\[ Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln \left( \frac{5.98h}{0.8w + t} \right) [\Omega] \]
Build a Team Work For Brain Storming

Synergy

Development = Electronics + Mechanics + Thermal Management + Engineering/PCB/Technologist

Better be a part of a Team
Than a group of people doing Team Work

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