ALTiumLIVE 2018:
The Benefits Gained by Using HDI Technology

Susy Webb
Design Science
Sr PCB Designer
San Diego
Oct, 2018
HDI/ Microvia – What’s the difference

- IPC: uVias are laser vias of generally 6 mil drill (150 microns) or smaller
- HDI is the technology used with microvias:
  - Smaller holes and padstacks than TH
  - Smaller traces and clearances
  - Thinner Dielectrics
  - Finer aspect ratios
  - Etc.
When to make the jump to HDI:

- IC packages may need it – either high pin count or fine pitch uBGAs (.65mm and below)
- Large parts with lots of connections
- Lack of room - Small physical board size
- Using minimum holes and line widths/spaces and still not enough room for all
- Amount of time needed/allowed to design the board
- When uVias will add other needed benefits
Benefits

What HDI can Offer

- Increased design flexibility
- Theoretical Cost equality
- Improved reliability – HDI tested as the most reliable for organic substrates*
- Better for EMI and signal integrity*
- More creative fanout possibilities for all parts
- Efficient signal transition from layer to layer
- Often can be manufactured worldwide – large market for fab

*Happy Holden – “HDI/Microvia Technologies”, PCB East 2009
### Possible cost equality - Price/Density Comparison

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<th>B: HDI BLIND</th>
<th>C: HDI BL/BURIED VIA</th>
<th>D: 1BU BLIND</th>
<th>E: 2BU BLIND</th>
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RCI = Relative cost index, DEN = Pins per sq. in.

Picture reprinted from Happy Holden
HDI may cost more, but fewer Bd Layers may make up for it

- Example goes from 16 layers TH and BB to 12 layers w/HDi
- Much better for hole aspect ratios

Part of a slide from "Happy Holden – "What you need to learn to gain 3X to 4X higher Layout Density"
HDI may cost more, but smaller board size may make up for it

- Good if small physical board size needed
- Less board material needed
- Smaller board is easier to panelize

*Happy Holden – “HDI/Microvia Technologies”, PCB East 2009*
**Routing Efficiencies per type of board**

A measure of the total # of traces vs the total number possible (efficiency %)

<table>
<thead>
<tr>
<th>Design Scenario</th>
<th>Conditions</th>
<th>Efficiency (%)</th>
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<tr>
<td>Rigid Thru-Hole</td>
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<td>Rigid Thru-Hole and SMT</td>
<td>2 Sided Blind Vias*</td>
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<tr>
<td><strong>2 layer HDI Structure</strong></td>
<td>*</td>
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<tr>
<td><strong>4 layer HDI Structure</strong></td>
<td>With Blind/Buried Vias*</td>
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<td><strong>6 Layer HDI Structure</strong></td>
<td>With Blind/Buried Vias*</td>
<td>up to 75%</td>
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* = gridless CAD system

2 layer means 2 layers of Microvias

Reprinted from www.Merix.com
HDI may cost more, but can improve routing on all routing layers

- uVias depth allows more internal signal routing, and uVia size allows for more external routing

<table>
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<tr>
<th>TH 1mm (.0393”) pitch</th>
<th>HDI 1mm (.0393”)</th>
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<td>.5mm pad (@ .020”)</td>
<td>.25mm pad (@ .010”)</td>
<td>.25mm pad (@ .010”)</td>
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<td>.25mm hole (@.010”)</td>
<td>.125mm hole (@.005”)</td>
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<td>.1mm lines and spaces (@.004”)</td>
<td>.1mm lines and spaces (@.004”)</td>
<td>.076mm lines and spaces (@.003”)</td>
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</table>
uVia Depth and Board Thickness

- HDI size works well with smaller aspect ratio for layer thicknesses
- Smaller pads/holes take up less room
- TH aspect ratio generally 10:1 up to 12:1
- HDI aspect ratio generally 0.5:1 up to 0.7:1

Aspect Ratio = A) Board (or layer) Thickness divided by B) Drill Diameter
Thin boards – Thin layers – Thin copper

- The thinner dielectrics used with HDI can easily make thinner boards or many layers, if desired
- Even very thin dielectrics used (.002” or less)
- Thin dielectrics may lead to thin trace widths for impedance control
- Thinner copper thickness to start is recommended for trace width/spacing of below 3/4 due to etch compensation
Benefits

Thinner copper will allow for finer spacing, meaning more routes in same area possible

- Better efficiency = more traces/channels/boulevards
- Fewer routing layers needed

4/4 = 10 traces 3/3 = 12 traces
Benefits

Various possibilities for signal flow layer to layer without blocking other busses

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<tr>
<th>Layer</th>
<th>BUS #1</th>
<th>BUS #2</th>
<th>BUS #3</th>
<th>Critical Signal group #1</th>
<th>Critical Signal group #2</th>
<th>Power and Ground</th>
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<td>layer 10 - Signal w/ poured gnd</td>
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HDI Good for SI and EMI

- Because dielectric layers are thinner, traces closer to return planes
- Improved containment of energy fields
- Possibly better for amount of separation for differential pairs
- HDI external layers are often flooded plane - also good for EMI
- Allows planes to be close together
- Good for inter-plane capacitance
Benefits

Power Delivery

- Larger power/ground copper area under BGAs with HDI also means better inter-plane capacitance and potentially better power delivery
More routing on internal layers

- More signals benefit from routing on inner layers – good for signal integrity, trace shape, impedance control
Benefits

No Via Stubs

- uVias only go where needed
- No controlled depth/backdrilling necessary
- No backdrill obstructions/clearance
- Reduced inductance in via barrel

Pictures of ‘Backdrilled’ TH vias from Netex-0 “Extracting Geometry, Nets, and Components from ODB++”
uVIA in PAD better than TH Via in Pad

- SM for uVia is within the SM for pad so no extra SM opening needed as in dog bone
- Reduced inductance – connection is made right from ball to pad to via (w/o dog bone) and down to other layers.
Via in Pad also means smaller antipad openings to avoid for routing return

- Signals can route slightly closer to pads
Benefits

An offset uVia grid can add extra routes

- Helps any size part be more routable
- HDI vias can be centered in, offset from, or tangent to surface mount pads to set up routing channels
HDI Routing Channels Improve Efficiency

- Channels might be set up very differently to fan out a small, very fine pitch part vs a large or very fine pitch part
- Small parts may just need a path for all signals
HDI can make difficult parts routable

- Ability to fanout large, high pin count packages
- No way to route with through hole
- Or device would need too many TH routing layers
The Advantage of Channeled Fanouts

With good fanout patterns, you can effectively reduce the size of a large BGA array for routing.

With HDI, 1760 pins effectively reduced 41% to 1024.
uVias are not just for BGAs

- Via in pad can also help move parts close together
- Signals may be shorter and timing better
- Possibly smaller board as well
Benefits

When already on the board, uVias can be used in congested areas to lead signals out of BGA to an open area, and from there to TH or buried vias (.5mm part)
Benefits

Finer pitched parts can be used with HDI

- Some of the new parts are only available in small BGA packages
- Other fine pitch devices have very little room for all the large TH vias needed nearby

0.4mm BGA

0.35mm BGA
Some parts are just complex to route with TH vias
Benefits

Some parts are just complex to route with TH vias

- uVias would help with ESD routing
- uVias would help with differential routing on newer style ICs

TI_TS3USB30ERSWR
Some parts would benefit from using uVias

- Here, uVias help diff pairs move to inner layer, closer, & away from tab
Some boards or areas would benefit from uVias because of P&R density
Copper filled/planarized uVias allow for active parts to easily be placed on both sides of the board

- Easy to fan out parts on their ‘own’ layers
HDI Provides the largest variety or stackup possibilities

- Via patterns can stack and stagger through many layers
HDI can affect Thermal Management

- Consider thermal transfer when building stack
- The primary heat transfer is accomplished through conduction
- The tighter we place parts, the more heat
- The smaller parts often produce more heat
- Solid copper fill in uVias helps to improve heat transfer layer to layer
- Newer thin materials may also improve thermal performance*

*Happy Holden “HDI’s Beneficial Influence on High Frequency Signal Integrity”
Benefits

Flatter Weave Materials Available for HDI

- HDI’s spread material may be helpful to all signals’ quality – particularly HS or differential pairs
**Design for low cost**

- Keep to Type I or Type II, if possible – fewest laminations
- Use least depth of uVias – no skip vias
- When changing layers, staggered uVias are easier to produce than stacked
- If HDI is used on the board, it usually does not cost extra to use in many other places
- You can add microvias to a through hole board…. But it’s still a TH board, just more expensive*

*Happy Holden in “Current PCB Cost Adders”*
Fabrication Issues

- Get fabrication involved early!*
- **Check with your fabricator** for his norms before starting a board - capabilities, up-charges, turn times, etc.
- Think about fabrication yield… HDI may cost a bit more, but that may beat the cost of a TH board that is difficult for the designer to design and/or for the fabricator to build!
- **Consider what is most cost effective from a DFM point of view**
Thank you!

Susy Webb
DesignScience@ymail.com
Benefits to Board
<table>
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Many designers understand the help that HDI technology can give to the **fanout of a BGA**, but there are many other benefits to consider as well. Some may feel like uVias may be cost **prohibitive**, so we will talk about how the technology can affect the general efficiency of a board, counteracting that cost. The **routing and stackup possibilities** expand rapidly with HDI providing new resources, and we will discuss how it provides some true **benefits for signal integrity and EMI** too. And while some parts are fairly **awkward to route with through hole vias**, they can be much easier to design with uVias. All this and a few helpful manufacturing tips will be discussed in this presentation.
Efficient signal transition from layer to layer

Here, a Plan with ‘rough-in’ routing for a BGA with several types of vias

- Type III stack
Design Priorities – What is most needed on the board. Will HDI help with that?

- Major amounts of routing
- SI and EMI control
- Good power delivery
- Signals, power and ground flowing throughout board
- Low Cost
- Board thickness issues
- ALL of the above
HDI can affect Embedded Passives

12 layer Type I HDI

1. SMT/Test Pins
2. GND
3. PWR
4. Sig_2
5. Sig_3
6. GND
7. Sig_4
8. Sig_5
9. GND
10. Sig_6
11. PWR
12. SMT/GND Test

Benefits

*Happy Holden – “HDI/Microvia Technologies”, PCB East 2009
Cost equality

Price/Density Comparison

- Possible cost equality - talk with your vendor about everything that your board will need
- 8 layer TH board is the base for comparison
  - An 8 layer TH board may reduce to a 4 layer Type I board for lower RCI
  - A 14 layer TH board may reduce to a 8 layer Type II board for lower RCI
Benefits to Board
Benefits to Board
The Benefits Gained by Using HDI Technology on Boards

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Fairfield Geotechnologies
Houston, Texas

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<td>DEN 145</td>
<td>RCI 19.17</td>
<td>DEN 620</td>
<td>RCI 21.21</td>
<td>DEN 1500</td>
<td>RCI 19.09</td>
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<td>RCI 21.69</td>
<td>DEN 660</td>
<td>RCI 23.73</td>
<td>DEN 1700</td>
<td>RCI 21.89</td>
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<td>RCI 22.79</td>
<td>DEN 160</td>
<td>RCI 23.96</td>
<td>DEN 700</td>
<td>RCI 25.94</td>
<td>DEN 1900</td>
<td>RCI 24.18</td>
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<td>DEN 180</td>
<td>RCI 25.91</td>
<td>DEN 740</td>
<td>RCI 28.60</td>
<td>DEN 2100</td>
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<td>DEN 200</td>
<td>RCI</td>
<td>DEN</td>
<td>RCI</td>
<td>DEN</td>
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</tr>
</tbody>
</table>

RCI = Relative cost index, DEN = Pins per sq. in.

Picture reprinted from Happy Holden
HDI may cost more, but fewer Bd Layers may make up for it

- Example goes from 16 layers TH and BB to 12 layers w/HDl
- Much better for hole aspect ratios

Part of a slide from *Happy Holden – “What you need to learn to gain 3X to 4X higher Layout Density”*
Benefits to Board

HDI may cost more, but smaller board size may make up for it

- Good if small physical board size needed
- Less board material needed
- Smaller board is easier to panelize

Before – 12 layer

After HDI - 8 layer

*Happy Holden – “HDI/Microvia Technologies”, PCB East 2009
Routing **Efficiencies** per type of board

A measure of the total # of traces vs the total number possible (efficiency %)

<table>
<thead>
<tr>
<th>Design Scenario</th>
<th>Conditions</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rigid Thru-Hole</td>
<td>Gridded CAD</td>
<td>30%</td>
</tr>
<tr>
<td>Rigid Thru-Hole and SMT</td>
<td>With or W/O Back Side Passives</td>
<td>35.50%</td>
</tr>
<tr>
<td>Rigid Thru-Hole and SMT</td>
<td>With Back Side Active Components</td>
<td>30.45%</td>
</tr>
<tr>
<td>Rigid SMT Only</td>
<td>With Back Side Active*</td>
<td>up to 55%</td>
</tr>
<tr>
<td>Rigid Thru-Hole and SMT</td>
<td>1 Sided Blind Vias*</td>
<td>up to 60%</td>
</tr>
<tr>
<td>Rigid Thru-Hole and SMT</td>
<td>2 Sided Blind Vias*</td>
<td>up to 65%</td>
</tr>
<tr>
<td>2 layer HDI Structure</td>
<td>*</td>
<td>up to 70%</td>
</tr>
<tr>
<td>4 layer HDI Structure</td>
<td>With Blind/Buried Vias*</td>
<td>up to 80%</td>
</tr>
<tr>
<td>6 Layer HDI Structure</td>
<td>With Blind/Buried Vias*</td>
<td>up to 75%</td>
</tr>
</tbody>
</table>

* = gridless CAD system

2 layer means 2 layers of Microvias  

Reprinted from www.Merix.com
HDI may cost more, but can improve routing on all routing layers

- uVias depth allows more internal signal routing, and uVia size allows for more external routing

**TH 1mm (.0393”) pitch**
- .5mm pad (@ .020”)
- .25mm hole (@.010”)
- .1mm lines and spaces (@.004”)

**HDI 1mm (.0393”)**
- .25mm pad (@ .010”)
- .125mm hole (@.005”)
- .1mm lines and spaces (@.004”)

**HDI 1mm (.0393”)**
- .25mm pad (@ .010”)
- .125mm hole (@.005”)
- .076mm lines and spaces (@.003”)
**Benefits to Board**

**uVia Depth and Board Thickness**

- HDI size works well with smaller aspect ratio for layer thicknesses
  - Smaller pads/holes take up less room
  - TH aspect ratio generally 10:1 up to 12:1
  - HDI aspect ratio generally 0.5:1 up to 0.7:1

Aspect Ratio = A) Board (or layer) Thickness divided by B) Drill Diameter
Thin boards – Thin layers – Thin copper

- The thinner dielectrics used with HDI can easily make thinner boards or many layers, if desired
- Even very thin dielectrics used (.002” or less)
- Thin dielectrics may lead to thin trace widths for impedance control
  - Thinner copper thickness to start is recommended for trace width/spacing of below 3/4 due to etch compensation
Benefits to Board

Thinner copper will allow for finer spacing, meaning more routes in same area possible

- Better efficiency = more traces/channels/boulevards
- Fewer routing layers needed

4/4 = 10 traces  3/3 = 12 traces
Various possibilities for signal flow layer to layer without blocking other busses
Benefits to Board

HDI Good for SI and EMI

- Because dielectric layers are thinner, traces closer to return planes
  - Improved containment of energy fields
  - Possibly better for amount of separation for differential pairs
- HDI external layers are often flooded plane - also good for EMI
  - Allows planes to be close together
  - Good for inter-plane capacitance
Benefits to Board

Power Delivery

- Larger power/ground copper area under BGAs with HDI also means better inter-plane capacitance and potentially better power delivery
Benefits to Board

More routing on internal layers

- More signals benefit from routing on inner layers – good for signal integrity, trace shape, impedance control
Benefits to Board

**No Via Stubs**

- uVias only go where needed
- No controlled depth/backdrilling necessary
- No backdrill obstructions/clearance
- Reduced inductance in via barrel

Pictures of ‘Backdrilled’ TH vias from Netex-0 “Extracting Geometry, Nets, and Components from ODB++”
Benefits to Board

**uVIA in PAD better than TH Via in Pad**

- SM for uVia is within the SM for pad so no extra SM opening needed as in dog bone
- Reduced inductance – connection is made right from ball to pad to via (w/o dog bone) and down to other layers.
Via in Pad also means smaller antipad openings to avoid for routing return

- Signals can route slightly closer to pads
An offset uVia grid can add extra routes

- Helps any size part be more routable

- HDI vias can be centered in, offset from, or tangent to surface mount pads to set up routing channels
HDI Routing Channels Improve Efficiency

- Channels might be set up very differently to fan out a small, very fine pitch part vs a large or very fine pitch part
- Small parts may just need a path for all signals

Benefits to Board

Reprinted with permission from BGA Breakouts & Routing by Charles Pfeil
HDI can make difficult parts routable

- Ability to fanout large, high pin count packages
- No way to route with through hole
- Or device would need too many TH routing layers

TI GTM (N2377) BGA with 2377 pins at 1mm pitch
The Advantage of Channeled Fanouts

With good fanout patterns, you can effectively reduce the size of a large BGA array for routing.

With HDI, 1760 pins effectively reduced 41% to 1024.

Reprinted with permission from BGA Breakouts & Routing by Charles Pfeil
uVias are not just for BGAs

- Via in pad can also help move parts close together
- Signals may be shorter and timing better
- Possibly smaller board as well
When already on the board, uVias can be used in congested areas to lead signals out of BGA to an open area, and from there to TH or buried vias (.5mm part)

Benefits to Board
Finer pitched parts can be used with HDI

- Some of the new parts are only available in small BGA packages
- Other fine pitch devices have very little room for all the large TH vias needed nearby
Benefits to Board

Some parts are just complex to route with TH vias
Some parts are just complex to route with TH vias

- uVias would help with ESD routing
- uVias would help with differential routing on newer style ICs
Some parts would benefit from using uVias

- Here, uVias help diff pairs move to inner layer, closer, & away from tab

Benefits to Board
Some boards or areas would benefit from uVias because of P&R density

Better picture?
Copper filled/planarized uVias allow for active parts to easily be placed on both sides of the board

- Easy to fan out parts on their ‘own’ layers
HDI Provides the largest variety or stackup possibilities

- Via patterns can stack and stagger through many layers
HDI can affect Thermal Mgt.

- Consider thermal transfer when building stack
  - The primary heat transfer is accomplished through **conduction**
  - The tighter we place parts, the more heat
  - The smaller parts often produce more heat
  - Solid copper fill in uVias helps to improve heat transfer layer to layer
  - Newer thin materials may also improve thermal performance*

*Happy Holden “HDI’s Beneficial Influence on High Frequency Signal Integrity”*
Flatter Weave Materials Available for HDI

- HDI’s spread material may be helpful to all signals’ quality – particularly HS or differential pairs.
Design for low cost

- Keep to Type I or Type II, if possible – fewest laminations
  - Use least depth of uVias – no skip vias
- When changing layers, staggered uVias are easier to produce than stacked
- If HDI is used on the board, it usually does not cost extra to use in many other places
  - You can add microvias to a through hole board…. But it’s still a TH board, just more expensive*

*Happy Holden in “Current PCB Cost Adders”
Fabrication Issues

- Get fabrication involved early!*
- Check with your fabricator for his norms before starting a board - capabilities, up-charges, turn times, etc.
- Think about fabrication yield... HDI may cost a bit more, but that may beat the cost of a TH board that is difficult for the designer to design and/or for the fabricator to build!
- Consider what is most cost effective from a DFM point of view
Thank you!

Susy Webb

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