THERMAL ANALYSIS & ELECTRICAL STRESS DERATING, INTEGRATED IN ALTUIM DESIGNER: A PROVEN WAY TO INCREASE PRODUCT RELIABILITY AND ROBUSTNESS
About BQR Company
Sample Design Errors
Stress Analysis and Rules
Simulation Flow in Altium
Simulation Input Data
Automated Schematic Review
Rapid and Precise Methods
Simplified Thermal analysis
Electrical Stress Derating Analysis
Reliability Predications
Other Reliability Analysis
Conclusions
About BQR

- A world leader in Quality, Reliability, Availability, Maintenance and Safety (QRAMS) Engineering for electronic and mechanical product/asset improving the products in the design stage
- Founded in Israel in 1989 as a RAMS Software development company for the EDA/MDA, PLM, CMMS, EAM and ERP (IIOT) market
- A team of expert Mathematicians, Electronic and Reliability engineers (BSc., MSc. & PhD.)
- Worldwide customers including leading global enterprises
- Experts in breaking any system down to components, and building up the QRAMS models for Optimal Reliability and Maintenance

Industries:

Energy, Power, Wind Farms, Aerospace, Defense, Automotive, Railways, Telecom, Oil & Gas, Utilities
And any industry that uses electronic and mechanical components
“fiXtress helps us accelerate our efforts to perform automated design reviews, electrical stress analysis and reliability prediction prior to PCB layout and manufacturing. It is both a time-saver and a productivity enhancer.”

Dr. Josh Liew, Reliability Program Manager, Baker Hughes (Altium User)
This presentation will show you how to prevent such cases in the schematic phase using Altium Designer.
Standard Design Flow

- **Schematic**
- **DRC, Visual Inspection**
- **PCB Layout**
- **Prototype Manufacturing**
- **Prototype Test**
- **Qualification Test**
- **Integration Test**
- **Customer**
- **Design Correction**
- **Root Cause Analysis**
- **Found Design Error**

- $10
- $100
- $1,000
- $10,000
- $100,000
- $1,000,000

$1,000
$10,000
$100,000
$1,000,000
fiXtress Design Flow

ODM Check gate for Design Quality
Original Design Manufacturer

Benefits:
- Saves time of schematic visual inspection
- Saves Design debug time
- Reduces Design Re-Spins
- Improves Documentation and Process

Dramatically reduces the need for Design Correction
Dramatically reduces the need for Root Cause Analysis
Almost Zero Errors Found
Return on Investment ROI: 10 when design errors are detected during schematic
• Statistics on 14 boards
• Design errors and stress errors
• ROI : 1 - 35

Reducing Product Time-to-Market based on Shortening the Design Cycle

January 28-31, 2019
At the Walt Disney Contemporary Resort, Orlando, Florida, USA

<table>
<thead>
<tr>
<th>Number</th>
<th>Item</th>
<th>PAD Quantity</th>
<th>Components quantity</th>
<th>Net quantity</th>
<th>Finding Errors(*)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Module 1</td>
<td>11238</td>
<td>1691</td>
<td>2315</td>
<td>129</td>
</tr>
<tr>
<td>2</td>
<td>Module 2</td>
<td>8825</td>
<td>1931</td>
<td>2666</td>
<td>51</td>
</tr>
<tr>
<td>3</td>
<td>Module 3</td>
<td>4318</td>
<td>10005</td>
<td>1172</td>
<td>6+35</td>
</tr>
<tr>
<td>4</td>
<td>Module 4</td>
<td>2870</td>
<td>751</td>
<td>749</td>
<td>3+82</td>
</tr>
<tr>
<td>5</td>
<td>Module 5</td>
<td>10169</td>
<td>1395</td>
<td>1139</td>
<td>2+17</td>
</tr>
<tr>
<td>6</td>
<td>Module 6</td>
<td>1190</td>
<td>286</td>
<td>299</td>
<td>3+2</td>
</tr>
<tr>
<td>7</td>
<td>Module 7</td>
<td>7215</td>
<td>1279</td>
<td>1781</td>
<td>24+12</td>
</tr>
<tr>
<td>8</td>
<td>Module 8</td>
<td>6450</td>
<td>1343</td>
<td>1390</td>
<td>21+66</td>
</tr>
<tr>
<td>9</td>
<td>Module 9</td>
<td>9480</td>
<td>979</td>
<td>2192</td>
<td>11+5</td>
</tr>
<tr>
<td>10</td>
<td>Module 10</td>
<td>1963</td>
<td>426</td>
<td>380</td>
<td>6+5</td>
</tr>
<tr>
<td>11</td>
<td>Module 11</td>
<td>6584</td>
<td>749</td>
<td>2014</td>
<td>4+23</td>
</tr>
<tr>
<td>12</td>
<td>Module 12</td>
<td>2657</td>
<td>157</td>
<td>941</td>
<td>1+24</td>
</tr>
<tr>
<td>13</td>
<td>Module 13</td>
<td>3318</td>
<td>697</td>
<td>895</td>
<td>9+3</td>
</tr>
<tr>
<td>14</td>
<td>Module 14</td>
<td>4365</td>
<td>1069</td>
<td>1158</td>
<td>11+50</td>
</tr>
</tbody>
</table>
Sample Design Errors
Design error sample

"Floating IC GND" rule #2

0.138 V > 0V
These power pins were not connected to the power rail.
This part of the design was copied to three other designs, resulting in the same issue.
Error message: Component TPS73201DRBR RefDes U52
Calculated input voltage at pin 3 is lower than the minimum allowed.

From the Data sheet, pin 3 should be 1.2 V

U52 output voltage should be 1.6V. The output voltage was calculated to be:
\[ V_{out} = 1.204 \times \left( \frac{R1(R804)+R2(R805)}{R2(R805)} \right) = 4.83V \]

Recommendation: R804 and R805 should be switched
**Error message:** Component FDV303N RefDes M3 Calculated voltage Vgs (12V) is greater than the rated voltage (8V)

The data sheet maximum value for VGS value is 8V.

<table>
<thead>
<tr>
<th>Absolute Maximum Ratings</th>
<th>FDV303N</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{DSS}</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>V_{GSS}</td>
<td>8</td>
<td>V</td>
</tr>
</tbody>
</table>

**Data sheet**
A high level on pin U1-40 cannot open the Q1 transistor due to a wrong R42 value

How it should work
• PB4 control the LED to be ON/OFF
• For LED to be ON, PB4 should 1 logic, (2.6V)
• For LED to be OFF, PB4 should 0 logic, (1.2V)
• But LED will never turn ON.

The reason why LED will never turn ON:
• For LED to be ON: Transistor Q1 should be ON, if Vb~0.6v
• But from resistors divider, the voltage is 2.6*(1k/11k)= 0.23v
• Vb; 0.23V < 0.6V
• Therefore transistor Q1 will be always OFF and LED will be OFF

Recommendation:
• Resistors value need to be adjusted.
When Q1 is switched OFF, the resistor divider between the internal pull-down resistor and R59 generates 1.052V, (“high” level).

How it should work:
• Transistor Q1 controls pin PB4 to be High or Low.
• If Q1 is ON, (Vb high), then PB4 should be a logic “low” level.
• If Q1 is OFF, (Vb low), then PB4 should be a logic “high” level.

The reason why PB4 will not receive correct logic levels:
• If Transistor Q1 is OFF (make PB4 as 1)
• Vcollector≈ 1.052V (fixtress calculations)
• The result of 1.052V is above 1.0V and below 2.3V, then U1-PB4 logic level is incorrect.

Recommendation:
• Resistors value need to be adjusted.
What is stress?

Derating:
25% from max load

Max Cable: 500Kg

Max Cable: 2,000Kg

After 10 times the cable will tear

After 1,000,000 times the cable will tear
Derating in Electronics
What is Reliability?

Failure Probability Vs. Temperature and Electrical Stress

Increasing stress even with low Temperature will result in 100% failure
PCB Power Reduction after Using fiXtress

Before: power was reduced

<table>
<thead>
<tr>
<th>System</th>
<th>Part Number</th>
<th>Part Name</th>
<th>Power Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>20130315</td>
<td>Controller Board</td>
<td>Before: 3.930 W, After: 3.267 W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>20130315</td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>20130315</td>
<td>SIM</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>20130315</td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>20130315</td>
<td>SIM</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>20130315</td>
<td></td>
</tr>
</tbody>
</table>

After: power was reduced
MTBF Improvement after Using fiXtress

Before

After design errors correction
BQR Schematic Review Methods

A. Schematic Rules

A1. Common

A2. Project based (Connectivity Verification)

A3. Chip Interconnection

B. Compliance with Electrical Specs

1. Compliance of calculated IC Output Current per pin with Specs (Not Failure Found)
2. Compliance of calculated IC Supply Voltage with Specs
3. Verification of Transistors and Diodes Operational functional modes
4. Compliance of IC Input Voltage per pin to Specs (Example: Feedback voltage of voltage regulators)
5. Compliance of IC Output Voltage per pin to Specs
6. Verification of IC operating Frequency according to Specs
7. Reverse polar capacitor detection
8. Correspondence of IC Digital Input Signal levels to Specs
9. Check if the IC Digital signal Input gets both logical levels (Low and High)
Integration Flow

- **BOM**
- **Net List**
- **PINs**
- **ICD**

**Schematic Design:**
- **ASR** Single Board
  - Avoid Errors causing high stress
  1. Common
  2. Connectivity Verification
  3. Chip Interconnection
  - Automated Schematic Review

- **Rapid** Single Board
  - Avoid Errors caused by high stress
  - Stress Simulation
  - Rules Based DC
  - Automated Schematic Review

- **Precise** Single Board
  - Avoid Errors caused by high stress
  - Stress Simulation
  - DC, AC & BUS Full Kirchhoff + Fourier
  - Automated Schematic Review

- **ASR** Multi Boards Integration
  - Schematic n
  - Schematic 2
  - Schematic 1

**fiXtress** Plug-in & Tool-kit
- Data Preparation
- MTBF Parts Count
- Net Name Generator

**Back Annotation**
- Stress Derating
  - Stress Derating Analysis
  - Parts Stress

**MTBF**
- MTBF Results Review

**Mini Thermal**
- ΔT Calculation
- Power Voltage Current

**Server fiXtress** Libraries

**MTBF Results Review**
Benefits

- Automated Schematic Review tool; Detects hidden design errors, driven by Electrical Stress, Reliability, Testability and Safety analysis
- Real simulation is done by using the ICD between PCBs for Multi Boards analysis.
- Ready to use 17 groups of design rules, each one has about 15 sub-groups (~200 rules)
- The user can easily define new design rules for different applications such as Testability, ESD and Safety (predefined 56 rules are ready to use)
- fiXtress runs all rules together and not one by one as used by the scripts
- Very fast and accurate results in minutes running hundreds of rules on a 100,000 pads PCB with 25,000 component
- Checks for every pin the applied actual voltage and current, that comes from a real stress simulation to comply with the components standards
- Prevents hidden design errors, the cause of NFF (No Failure Found) during service
- Advanced level of rules that can check group of signals & BUSs between chips
- Ready to use derating standards
- The user can create his own derating standards
- Detects all EOS (Electrical Over Stress) violations with Pareto, Overstress and Overdesign reports
- Contains simplified Thermal analysis that estimates the average temperature rise from the cold-plate, for accurate stress Derating
- Drives the actual power dissipation for 3D Thermal Analysis and Physics of Failure (PoF)
- Calculate the accurate MTBF base on real electrical and thermal stress
- MTBF prediction for all available standards
- Drives reliability data automatically to all RAMS analysis (FMECA, FTA, RBD, MTTR)
fiXtress Operation Overview
Integration with CAD & PLM Tools

EDA Schematic Capture

fiXtress Plug-In

fiXtress

Input Data Processing

Output Data Processing

Input Files: BOM Net-List Pin-Lib

Results Files: MTBF SDTA Errors Report

MTBF (Hours)

Before fiXtress

After fiXtress

MTBF vs. Temperature Temp °C

Input Data Processing

Output Data Processing

Integration with CAD & PLM Tools
Live Altium Designer Demo
### External Sources And Loads (ICD)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>J21 6</td>
<td>AFOX_INT_N</td>
<td>GRID</td>
<td>HIGH_3V</td>
<td>Voltage</td>
<td>DC</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>J21 9</td>
<td>AFOX_INT_N</td>
<td>GRID</td>
<td>HIGH_3V</td>
<td>Voltage</td>
<td>DC</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>J22 1</td>
<td>AFOX_INT_D</td>
<td>GRID</td>
<td>HIGH_25V</td>
<td>Voltage</td>
<td>DC</td>
<td>2.5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>P2 A</td>
<td>RS422_1_2P</td>
<td>RS422_1_2N</td>
<td>-</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>6 12</td>
<td>0.115</td>
<td>-</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>P2 A</td>
<td>Prox_SDA_RX_P</td>
<td>Prox_SDA_RX_N</td>
<td>-</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>1.5</td>
<td>3</td>
<td>1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>P2 A</td>
<td>AC_LVDS_1_2H_P</td>
<td>AC_LVDS_1_2H_N</td>
<td>-</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>5.18</td>
<td>0.36</td>
<td>100</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>P2 A</td>
<td>GL_MSYNC_UP</td>
<td>GL_MSYNC_DOWN</td>
<td>-</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>7</td>
<td>19</td>
<td>1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>P2 A</td>
<td>Pins_LV36</td>
<td>GRID</td>
<td>D510K_32.2v</td>
<td>Voltage</td>
<td>DC</td>
<td>32/2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>P2 B1</td>
<td>FAN_PWR</td>
<td>FAN_PWR_RST</td>
<td>-</td>
<td>Voltage</td>
<td>DC</td>
<td>32</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>P2 B1</td>
<td>A429_1_13P</td>
<td>A429_1_13N</td>
<td>-</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>5</td>
<td>10</td>
<td>0.1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>P2 B1</td>
<td>A429_1_17P</td>
<td>A429_1_17N</td>
<td>-</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>5</td>
<td>10</td>
<td>0.1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>P2 B2</td>
<td>Prox_SDA_RX_N</td>
<td>GRID</td>
<td>Not Connected</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>1.5</td>
<td>3</td>
<td>1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>P2 B3</td>
<td>A429_1_25P</td>
<td>A429_1_25N</td>
<td>-</td>
<td>Voltage</td>
<td>Rectangular</td>
<td>5</td>
<td>10</td>
<td>0.1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

![Diagram](image_url)
### Input Data, Clock Frequency

#### Assign Frequency

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Net Freq [MHz]</th>
<th>IC Freq [MHz]</th>
<th>RefDes</th>
<th>PIN Num</th>
<th>Part Num</th>
<th>Cat. Num</th>
<th>Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>A016_CLK1_T_A</td>
<td>1</td>
<td>100.25</td>
<td>U11</td>
<td>6</td>
<td>531FB100X250DG</td>
<td>000990454F</td>
<td></td>
</tr>
<tr>
<td>A016_CLK1_T_B</td>
<td>1</td>
<td>100.25</td>
<td>U11</td>
<td>4</td>
<td>531FB100X250DG</td>
<td>000990454F</td>
<td></td>
</tr>
<tr>
<td>PCI_CLK1_T</td>
<td>1</td>
<td>66</td>
<td>U170</td>
<td>3</td>
<td>CY2305CSX1-1H</td>
<td>00078377F</td>
<td></td>
</tr>
<tr>
<td>POL_CLK2_T</td>
<td>2</td>
<td>66</td>
<td>U170</td>
<td>2</td>
<td>CY2305CSX1-1H</td>
<td>00078377F</td>
<td></td>
</tr>
<tr>
<td>PCB_FPGA_CLK0_T</td>
<td>2</td>
<td>66</td>
<td>U170</td>
<td>2</td>
<td>CY2305CSX1-1H</td>
<td>00078377F</td>
<td></td>
</tr>
</tbody>
</table>

#### IC components operating frequency

<table>
<thead>
<tr>
<th>RefDes</th>
<th>Internal Frequency [MHz]</th>
<th>Maximum Operational Frequency [MHz]</th>
<th>Percent Of Usage</th>
<th>Part Number</th>
<th>Group Name</th>
<th>Frequency Distribution Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>U155</td>
<td>-</td>
<td>42</td>
<td>100</td>
<td>NC7533P5X</td>
<td>IC Dig-Others</td>
<td>Open</td>
</tr>
<tr>
<td>U157</td>
<td>-</td>
<td>100</td>
<td>100</td>
<td>MAX05901SGA</td>
<td>IC General</td>
<td>Open</td>
</tr>
<tr>
<td>U166</td>
<td>-</td>
<td>100</td>
<td>100</td>
<td>SN755VHD1781DG4</td>
<td>IC Dig-Others</td>
<td>Open</td>
</tr>
<tr>
<td>U167</td>
<td>-</td>
<td>100</td>
<td>100</td>
<td>SN755VHD1781DG4</td>
<td>IC Dig-Others</td>
<td>Open</td>
</tr>
<tr>
<td>U17</td>
<td>-</td>
<td>66</td>
<td>100</td>
<td>ADV7403BG75-110</td>
<td>IC General</td>
<td>Open</td>
</tr>
<tr>
<td>U170</td>
<td>66</td>
<td>133</td>
<td>100</td>
<td>CY2305CSX1-1H</td>
<td>IC General</td>
<td>Open</td>
</tr>
</tbody>
</table>

#### Pin List for RefDes 'U170', PartNum 'CY2305CSX1-1H' [IC General] - DIGITAL OUTPUT

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>POL_CLK2_T</td>
<td>OUTPUT</td>
<td>66</td>
<td>Rectangular</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>PCI_CLK1_T</td>
<td>OUTPUT</td>
<td>66</td>
<td>Rectangular</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>$VIN190</td>
<td>OUTPUT</td>
<td>-</td>
<td>Rectangular</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>$VIN187</td>
<td>OUTPUT</td>
<td>-</td>
<td>Rectangular</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>$VIN188</td>
<td>OUTPUT</td>
<td>-</td>
<td>Rectangular</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
The total current for the 5V supply is 1.077A = (0.5*2+0.077) and for 3.3V supply is 2.3A = (4*0.5+0.3). The power consumption with full load is 6.77W(24V)+8.5W(5V)+0.5W(-5v). Each component connected to J201/J202 consumes 6W, therefore the power dissipation upon the board is ~4W.
The two most common typical failures in the field are NTF and EOS:

- NTF = “No Trouble Found” (“NFF - No Failure Found”)
- EOS = “Electrical Over Stress”

NTF:
35%-70% of PCBs declared by field technicians as failed but are still functional and no failure is found in the lab. This dramatically increases the number of PCBs in the pipeline, causing manufacturers large losses. fiXtress includes special rules that can detect such errors based on the electrical stress simulation, saving time and capital.

EOS:
Material damage may occur when an electronic device is subjected to a power, current, voltage or temperature that is beyond the specified limits of the device.

- EOS affects product performance until the component burns. It is the leading cause of returns in components, IC and system failures during operation
- EOS causes damage to the materials, and product recalls, since this design error is embedded in all PCBs in the field.

fiXtress detects all EOS errors while increasing PCB reliability, and saving time and money
Total need: 20mA

When all IC11 - IC14 need the 5 mA current, and IC1 can supply only 12 mA, then the circuit fails. When checked in lab, No failure will be found.
Automated Schematic Review

Detect design errors before making stress analysis

ASR
Single Board
Avoid Errors causing high stress
1. Common Rules
2. Connectivity Rules
3. Chip Interconnection

Automated Schematic Review
Decoupling Capacitors Rule #11

Report

<table>
<thead>
<tr>
<th>Phase</th>
<th>Message Type</th>
<th>Message</th>
</tr>
</thead>
<tbody>
<tr>
<td>Decoupling Capacitors</td>
<td>Major</td>
<td>There is not enough decoupling capacitor quantity between power net 2N292 (power bus VCC) and ground net GND (ground bus GND BUS1) required qty=3, found qty=2.</td>
</tr>
</tbody>
</table>
Capacitor should be between 12 to 24 pF

Advanced Rule

Report

<table>
<thead>
<tr>
<th>#</th>
<th>Rule Number</th>
<th>Rule Group</th>
<th>Message</th>
<th>Severity</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>BGR_Crystal</td>
<td>The S2K515 ( thru PinName=G5C0; RefDes=U1, PinNum=41) net is connected to the GND net thru Extern Capacitor (RefDes=G4, PinNum=1), but that is not within value range</td>
<td>Major</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>BGR_Crystal</td>
<td>The S2K516 ( thru PinName=G5C1; RefDes=U1, PinNum=41) net is connected to the GND net thru Extern Capacitor (RefDes=G5, PinNum=1), but that is not within value range</td>
<td>Major</td>
</tr>
</tbody>
</table>
There should be a resistor connected to ground (data sheet requirement).

### Design Rule

<table>
<thead>
<tr>
<th></th>
<th>BGR_Output_Level</th>
<th>PinType</th>
<th>Bidir</th>
<th>Net</th>
<th>Short Connection</th>
<th>Severity</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GND</td>
<td></td>
<td>Not connect</td>
</tr>
</tbody>
</table>

### Report

<table>
<thead>
<tr>
<th>#</th>
<th>Rule Number</th>
<th>Rule Group</th>
<th>Message</th>
<th>Severity</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>1</td>
<td>BGR_Output _Level</td>
<td>The GND ( thru PinType=Bidir, RefDes=U4, PinNum=10 ) net is connected to 185 pads ( NetName=GND thru RefDes=C53, PinNum=1; NetName=GND thru RefDes=C54, PinNum=1; NetName=GND thru RefDes=C55, PinNum=1; and so on)</td>
<td>Minor</td>
</tr>
</tbody>
</table>
Resistor is not in range. Check again the pull-up value.

### Design Rule

<table>
<thead>
<tr>
<th>#</th>
<th>Rule Number</th>
<th>Rule Group</th>
<th>Message</th>
<th>Severity</th>
</tr>
</thead>
<tbody>
<tr>
<td>59</td>
<td>BQR_pull up</td>
<td>RS7</td>
<td>The mcu_wifi_cs (thru PinType=Input; RefDes=U2; PinNum=26) net is connected to the +3V3C net thru Extern Resistor (RefDes=RS7, PinNum=1), but that is not within value range</td>
<td>Minor</td>
</tr>
</tbody>
</table>
Rapid Electrical Stress Calculation

Precise Electrical Stress Simulation
Precise Simulations – Results Verification

DC Manual calculation (high state):

\[ R_{IN\_HIGH} = \frac{V_{SPL} - V_{OH}}{I_{OH}} = \frac{3.3 - 3.3 \times 0.879}{0.012} = 33.27\,\text{ohm} \]

\[ R_{T1} = R_{IN} + R_{430} = 33.27 + 30.1 = 63.37\,\text{ohm} \]

\[ R_{T2} = \left( R_{T1} \parallel R_{310} \right) = 63.37\,\text{ohm} \parallel 4.75\,\text{Kohm} = 62.54\,\text{ohm} \]

\[ V_X = \frac{V_{SPL} \times R_{LOAD}}{R_{LOAD} + R_{T2}} = \frac{3.3 \times 1\,\text{K}}{1\,\text{K} + 62.5} = 3.1V \]

\[ I_{R430} = \frac{V_{SPL} - V_X}{R_{T2}} = \frac{3.3 - 3.1}{62.5} = 0.032\,\text{mA} \]

DC Auto calculation (high state):

\[ \text{Same result} \]

\[ \text{U40} \]

\[ R_{in} \]

\[ 3.3V \]

\[ TDO \]

\[ 1\,\text{K} \]

\[ R_{load} \]

\[ \text{Same result} \]
Precise Simulations – Results Verification

Operational amplifier U14A works as a comparator. Vo (pin 1) can be approximately Vout-max or 0V. Vout-max is approximately 26.5V. Forward voltage of U11B is 1.35V. Current through R134 is calculated as follows:

\[
I_{R134} = \frac{(26.5 - 1.35)}{5.1\,Kohm} = 4.96\,mA
\]

Power dissipation is:

\[
P = 4.96^2 \times 5.1\,Kohm = 125\,mW
\]

Power dissipation is greater than the rated value of 63mW. By automatic calculation we get the same result:
Rapid & Precise Simulation Results Review

Check compliance to electrical specs based on stress simulation results
Sample Design Error
Zener D\text{U} is Connected In Reverse

Zener Diode should protect the circuit when Vbus is above 9V

The pin information

The Netlist assignment

State status:

wrong
Mini Thermal

Estimates the average temperature rise from the cold-plate

For accurate stress Derating, Thermal analysis estimates the average temperature rise from the cold-plate
Mini Thermal Module

Ta = 71°C

Results are similar to CFD thermal analysis
What Is Stress Derating?

- Stress in electronic parts may refer to Voltage, Power, Current and Junction Temperature.
- Derating increases the safety margin between part design limits and applied stresses, thereby providing extra protection for the part.
- By applying Derating for electronic components, their degradation rate is reduced. The reliability and life expectancy are increased.
Automated Calculated Electrical Stress Derating Parameters

<table>
<thead>
<tr>
<th>Component type</th>
<th>Applicable stress value calculated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Integrated Circuit</td>
<td>$T_j$, $P$, $F$, $I_{-out}$, $V_{-supply}$, $F$</td>
</tr>
<tr>
<td>Linear Integrated Circuit</td>
<td>$T_j$, $P$, $F$, $I_{-out}$, $V_{-out}$, $P_{-supply}$, $I_{-input}$</td>
</tr>
<tr>
<td>Thyristor and SCR</td>
<td>$T_j$, $P$, $I_{-on}$, $V_{-off}$, $I_{-Surge}$</td>
</tr>
<tr>
<td>Diode General Rectifier</td>
<td>$T_j$, $I_{-Forward}$, $V_{-Reverse}$, $I_{-Surge}$</td>
</tr>
<tr>
<td>Microwave Diode</td>
<td>$T_j$, $I_{-Forward}$, $V_{-Reverse}$, $I_{-Surge}$</td>
</tr>
<tr>
<td>Zener Diode</td>
<td>$T_j$, $V_{-peak}$, $I_{-peak}$, $I_{z_{av}}$</td>
</tr>
<tr>
<td>Transistor Bipolar</td>
<td>$T_j$, $V_{ceo}$, $I_{c}$, $I_{b}$, $V_{eb}$, $V_{cb}$</td>
</tr>
<tr>
<td>Field Effect Transistor</td>
<td>$T_j$, $V_{ds}$, $F$, $I_d$, $V_{gs}$, $V_{gd}$</td>
</tr>
<tr>
<td>Opto Device</td>
<td>$T_j$, $I_{-forward}$, $V_r$, $V_{ce}$, $V_c$</td>
</tr>
<tr>
<td>Resistor</td>
<td>$T_{mp}$, $P_{mp}$, $V_{mp}$, $C_{mp}$</td>
</tr>
<tr>
<td>Capacitor</td>
<td>$T_{mp}$, $V_{-Reverse}$, $I_{-Surge}$</td>
</tr>
<tr>
<td>Capacitor Tantalum Solid</td>
<td>$T_{mp}$, $V_{-Reverse}$, $I_{-Surge}$, $P_{w_{rip}}$</td>
</tr>
<tr>
<td>Inductive</td>
<td>$T_{mp}$, $V_{-Surge}$, $I_{-Surge}$, $I$, $V_{-Dielectric}$</td>
</tr>
<tr>
<td>Crystal</td>
<td>$I_{npw}$, $V_{sp}$, $V_{np}$, $T_{mp}$</td>
</tr>
<tr>
<td>Filter, RF and Microwave passive components</td>
<td>$I_{npw}$, $LO_{-Pw}$, $V_{-MP}$, $C_{MP}$, $T_{MP}$</td>
</tr>
<tr>
<td>Fuse</td>
<td>$T_{mp}$, $C_{mp}$, $V_{mp}$, $T_{mp}$</td>
</tr>
<tr>
<td>Lamp</td>
<td>$V_{mp}$</td>
</tr>
<tr>
<td>Connector</td>
<td>$T_{mp}$, $I_{npw}$, $V_{contacts}$, $V_{-Dielectric}$, $I_{b}$</td>
</tr>
<tr>
<td>Switch</td>
<td>$T_{mp}$, $P_{w_{cont}}$, $C_{mp}$, $I_{Load}$</td>
</tr>
<tr>
<td>Relay</td>
<td>$T_{mp}$, $V_{-coil}$, $C_{mp}$, $I_{Load}$</td>
</tr>
<tr>
<td>Hybrid Integrated Circuit</td>
<td>$T_{mp}$, $Pw$</td>
</tr>
<tr>
<td>Wires and cables</td>
<td>$T_{mp}$, $V_{mp}$, $I_{bw}$, $I_{sw}$</td>
</tr>
<tr>
<td>Tubes Microwave</td>
<td>$T_{mp}$, $Pw_{out}$, $Pw_{REF}$, $DC$</td>
</tr>
</tbody>
</table>

BQR can provide additional parameters upon request
MTBF Prediction

Calculate the MTBF of each PCB, and for the entire system
MTBF Prediction: Mean Time Between Failures

Prediction methods:

**Mil-HDBK-217-F2 & G**: Defense, Aerospace & any mission critical usage
**Telcordia Ver.3**: US Telecom
**FIDES**: Airbus
**IEC-62308**: French Telecom
**SN-29500**: Industry

The MTBF prediction result will increase by 50% after using fiXtress.
Reliability & System Safety Analysis Flow & Tasks from Component, Function, PCB, Box, sub-system, System up to Asset or Fleet Level

- **FMECA**: Build Components / Functional Failure Modes Catalog for Criticality, Safety & Testability Analyses
  - Functional breakdown
  - Failure Modes assignment
  - Next Higher Effect assignment
  - Severity Classification

- **Testability**: Define BIT concept & Tests to calculate BIT Coverage and Isolation
  - Assign for each Failure Mode the Relevant Built-In-Test (BIT)

- **FTA**: Build the Failure Modes Combinations Tree for System Safety Analysis
  - Build for each Safety Event the possible causes
  - Top-Down Assignment of Logical gates

- **RBD**: Build Redundancy model for System Availability Calculations
  - Assignment of required blocks / functions for a mission
  - Define the blocks / functions redundancy model

---

**fiXtress Boards Results**
- PCB n
- PCB 2
- PCB 1

**CARE Libraries**
Conclusions

- fiXtress™ & CARE® are the leading tools for EDA engineers
- Integrated with Altium Designer, makes it easy to use in the schematic phase
- High usability and ROI
- Reduce PCBs power dissipation (Green)
- Increases products robustness and reliability
- Reduces the design process time and Time To Market
- Cuts design process costs