AltiumLive 2017:
Creating Documentation for Successful PCB Manufacturing

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Agenda

1. Complexity & Cost
2. Thinking Outside the Board
3. Key Fabrication Requirements & Design Guidelines
4. Documentation Requirements
5. Demo
6. 20+ Common Technical Queries
1) **Manufacturing Panel Utilization** (how many PCBs fit on the master panel)

2) **Performance Class** (IPC-6012D Class 2 vs 3)

3) **Layer Count** (total number of required cores) \#cores = (#Layers-2)/2

4) **Number of Lamination Cycles** – each cycle requires lam/drill/plate/etch est.+25% per lam cycle

5) **Design Complexity** and whether the requirement is STANDARD (green), ADVANCED (yellow), or Engineering (red) capability
   - *Line Widths and Feature Spacing*
     - 4/4mil STD, 3/3mil +23-30%, 2.5/2/5 +50%
   - *Controlled Impedance (CI) tolerance*
     - 10%CI STD, 7%CI +20%, 5%CI +30% (if process-capable)
   - *Drilled Hole Size (Aspect Ratio = PCB Thickness: Drill Diameter)*
     - 25K drills/panel STD, extra 10K +1-2%, +15-20% drills < 8mil
   - *Overall PCB Thickness (Equipment Limitations)/ Aspect Ratios*
   - *Annular Ring Requirements (Registration Capabilities)*
   - *Copper Weights (Cost, Availability, and impact on Etching)*

6) **Type of dielectric Material**

7) **HDI/High Technology** (via-in-pad, buried capacitance)

8) **Process Yield** (often a Hidden Cost!)
Thinking Outside the Board

- Form, Fit & Function of the Assembly determine Dimensions, Thickness, and Connector & Mounting Hole locations
- Smallest Component pad size/pitch/density drive design complexity, technology, # of processes, and PCB cost
  - Fan-out of total pins determine the stack-up
    - number of layers, lamination cycles, and smallest features such as min linewidths/spaces, drills, and pads
    - HINT: Once outside the devices, design the rest of the features as large as possible to increase yields
- Surface Finishes versus shelf life, handling & application: HASL, LF-HASL, ENIG, OSP, ImSn, ImAg, Enepig
- Material – high speed, RF, and high temp materials are more expensive
- Protection of Vias-in-pad during assembly soldering
  - Cu-cap plated filled vias are 30% more expensive
  - Tented vias and solder mask plugs are inaccurate and may leave openings for chemical entrapment during solder
- PCB Technical difficulty – which fab site/s fit?
- Fabricator Stack-up & Design Guidelines for Site / Technology
- Fab Panel Utilization
  - Assembly Panels (Arrays) with rails, and how they fit multiple-up on the fabrication panel
- Assembly Requirements
  - Rails for conveyance
  - Stability of array
  - Over-Size arrays are limited by SMTA platforms, such as solder paste printers
- DFX (Design for Fabrication, Assembly, & Test); Follow the KISS (Keep It Super Simple) principle
- Migration path prototype (local) to mass production (Asia)
Outside the Board and Down the Assembly Line?

Does High V require special material?

How will this go down the line?

How many up on an array for SMT?  
Rails?  
Panel utilization killer?

What do we do about the overhanging parts during assembly?

Can a vision system read a leading cut-out edge?

Shock to the overhanging part solder Joints during operation?
Plan Ahead for Assembly
Excellent Panel Utilization

- PCB or array
- PCB
- PCB
- PCB

Total usable area 371 in\(^2\) total
Circuit area (including assembly rails) 300 in\(^2\)
\textbf{81\% panel utilization}

Add 0.5” rails to the long sides, and we reduce the panel to 2-up

Poor Panel Utilization

- PCB
- PCB
- PCB
- PCB

Total usable area 371 in\(^2\) total
Circuit area (including assembly rails) 187 in\(^2\)
\textbf{50\% panel utilization}

PCB COST = 2X
Design for Excellence, DFX:

• **Utilize Industry Standards**
  - Refer to IPC 2221 Generic Standard on Printed Board Design

• **Design for Fabrication, Assembly, & Test**
  - For complex designs, obtain a preliminary vendor stack-up before starting to route
  - Use min lines/spaces, drills/pads, and other clearances specified by fabricator
  - Design within Standard **GREEN** – not Advanced or Engineering - capability columns
    - Specify in Fab Notes when there are excessive requirements, such as small via/pad or line/space dimensions
  - Plan min component clearance of 0.200” - 0.300” from PCB edges, or rails will be needed
    - Specify on Fab & Assembly Drawings if space between PCBs is required for over-hanging components
  - Assure Top/bottom side BGAs are not mirrored or overlapped (can’t x-ray the balls)
  - Understand and properly specify via protection of off-set vias and via-in-pad designs
  - Keep test point, component, and wire bond pads from staking, BGA underfill, and other epoxies that may outgas and contaminate them
  - Design Test points for easy access at bare board pre-planning to assure sufficient coverage
  - Use thermals to promote through-hole solderability and inhibit SMT device tomb-stoning
DFX Human Resources:

- Electrical & Mechanical Design Engineers
- PCB Designers
- Test Engineers
- Process Engineers
- Quality Engineers
- Commodity Managers
- Suppliers
  - Field Applications Engineers
- Contract Manufacturers or OEM Manufacturing
- Valor NPI DFM Tool User
5 Best PCB Design Practices

• Optimize Assembly-ready PCB Dimensions for Material Best-fit

• Evaluate and Confirm the Most Complex Design Attributes and Prelim Stack-up

• Define Migration Path from Prototypes to Final Fabrication and Approve Stack-up with Final Fabrication Site/s

• Design and Document in Accordance with Standard Capability DFM Guidelines for Final Fabrication Site/s
  • Remember to create a .pdf Fabrication Drawing for Downstream Users

• Avoid Common Design Errors through knowledge and proof-reading
Key Fabrication Requirements that Affect Design Minimums

• **Symmetric** stack-ups (mirror images from the center out)
  • Lamination pressure
  • Flatness
  • Warp (bow & twist)

• **Aspect ratio (ratio of thickness to drill diameter, > 10:1 for through-holes)**
  • Ability to effectively plate Cu inside through and blind holes

• **Minimum drill to copper (avoid shorts and CAF, > 8mil)**
  • Required due to misregistration of materials and processes
    • Layer to Layer +/-3mil
    • Front to back imaging +/-2mil
    • Drill to drill +/-3mil
    • Drill to copper +/-2mil
    • Material shrinkage after etch requires compensation

• **Annular ring, Classes 1, 2 (90degree break-out) and 3 (min a/r 2mil outer, 1mil inner)**
  • Dependent on hole to pad size
  • Required due to misregistration

• **Outer/Plated layer thicknesses include base Cu foil plus thickness of plated Cu**
  • VIPPO adds an extra layer of plating to base Cu foil; may require slight increase in linewidths on outer layers
DFM Guidelines: Stack-up Symmetry

• With BGA devices prevalent in today’s designs, flatness is critical
• Symmetry ensures minimal warpage or residual stresses in the final product
• Should be symmetrical about the Z-axis, including layer copper, prepregs, and cores
DFM Guidelines: Aspect Ratio

Aspect Ratio = Ratio of Thickness to Drill bit diameter

Example 1. Mechanically drilled through hole that will be used to penetrate the entire thickness of the PCB or a through hole that will be used in a mechanically drilled sub-lamination used to form blind or buried vias. In this configuration the depth of the hole is measured from the surface of the external copper layers. In this case if the hole diameter was 0.010” and the depth was 0.093” the Aspect Ratio would be 9.3 to 1.

Max PTH Aspect Ratio: 10 to 1

Example 2. Laser drilled microvias are a controlled depth hole that terminates on a copper layer. As a result the depth of the hole is calculated from the top of the terminating layer to the top of the copper foil layer on the hole entrance. In this case if the hole diameter was 0.006” and the depth was 0.003” the Aspect Ratio would be 0.5 to 1.

Max Blind Aspect Ratio: 0.75 to 1

Unintended Consequences: Thin or no plating in the center of a PTH; thin/weak plating/bond in microvias
DFM Guidelines: Aspect Ratio, special cases

- Aspect ratio is the ratio of overall thickness to drill size but is not a universal indicator of capability.
- Related to how easily the hole walls can be plated with Cu
- Examples (All 10:1 Aspect Ratios)
  - 120 mil (3mm) thick PCB with 12 mil (0.3mm) drill – STANDARD
  - 80 mil (2mm) thick PCB with 8 mil (0.2mm) drill - ADVANCED
  - 60 mil (1.5mm) thick PCB with 6 mil (0.15mm) drill - ENGINEERING

<table>
<thead>
<tr>
<th>Aspect Ratio</th>
<th>Standard</th>
<th>Advanced</th>
<th>Engineering</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.006&quot; drill</td>
<td>green</td>
<td>6.5:1</td>
<td>10:1</td>
<td>14:1</td>
</tr>
<tr>
<td>0.008&quot; drill</td>
<td>yellow</td>
<td>8:1</td>
<td>10:1</td>
<td>12:1</td>
</tr>
<tr>
<td>0.010&quot; drill</td>
<td>yellow</td>
<td>10:1</td>
<td>12:1</td>
<td>16:1</td>
</tr>
<tr>
<td>0.012&quot; drill</td>
<td>yellow</td>
<td>10:1</td>
<td>14:1</td>
<td>18:1</td>
</tr>
<tr>
<td>0.0135&quot; drill</td>
<td>yellow</td>
<td>10:1</td>
<td>16:1</td>
<td>20:1</td>
</tr>
</tbody>
</table>

Always understand the context of a fabricator’s maximum aspect ratio capability listing
DFM Guidelines: Minimum Drill to Copper

**Standard (Mechanical Drills) = 0.008” (200 µm) Drill-to-Copper**

- Imaging - Front-to-Back = +/- 0.002” (50 µm)
- Lamination - layer-to-layer registration = +/- .003” (75 µm)
- Drill - Drill tolerance = +/- 0.003” (75 µm)

**Total Tolerance = 0.008” (200 µm)**

**Advanced (Mechanical Drills) = 0.0065” (165 µm) Hole-to-Copper – NOT ACCEPTED in ASIA**

- Imaging - Front-to-Back = +/- 0.001” (25 µm)
- Lamination - layer-to-layer registration = +/- .003” (75 µm)
- Drill - Drill tolerance = +/- 0.002” (50 µm)

**Total Tolerance = 0.006” (150 µm)**
DFM Guidelines: Minimum Drill to Copper

Hole-to-Copper (mechanical through-holes)

- **Annular Ring**: 0.005” (125 µm)
- **0.018” (508 µm) pad**
- **0.008” (254 µm) drill**
- **0.004” (100 µm) Trace**
- **0.004” (100 µm) Space**

- **>0.008” (204 µm) hole-to-copper**
- **0.004” (100 µm) Space**
- **0.008” (200 µm) minimum hole-to-copper should be utilized**

0.65 mm BGA
Internal Layer

**Through-hole Vias**

- **0.016” (400 µm) via pad**
- **0.008” (200 µm) drill**
- **0.003” (75 µm) trace**
- **0.0033” (83 µm) space**

**0.0073” (185 µm) drill-to-copper**
**Violates hole-to-copper min**
**Break-out allowed**
**Requires additional Engineering $$$$$**

**Thickness of 0.028” (0.711 mm) - 0.062” (1.575 mm)**
**Aspect Ratio 7.75:1**
DFM Guidelines: Annular Rings

**External annular ring** is measured from the inside of the plated through hole barrel to the edge of the land pad
- Class 2 = 90 degree break-out
- Class 3 = 2 mil minimum annular ring

**Internal annular ring** is measured from the hole barrel to the edge of the land pad
- Class 2 = 90 degree break-out
- Class 3 = 2 mil minimum annular ring

Non-Teardrop pad

Teardrop pad to maintain required minimum trace connection when breakout is allowed

IPC 6012B Breakout definition

A = 1.414 x Radius of PTH
B = Diameter of PTH
Worst case registration allowed by IPC Class II

Minimum annular Ring 1.969 mil

Larger pad than Class II to allow For registration

Minimum annular Ring 0.984 mil

Worst case registration allowed by IPC Class III
Minimum Drilled Hole To Copper & Minimum Class II Pad

- Internal pad designed for tangency
- Drilled hole to copper of 8 mils
- 3 mil space maintained

- Internal pad designed minimum with breakout
- Drilled hole to copper of 7 mils
- 3 mil space can be violated
- Design is too tight for excellent reliability or yield
### Mechanical Drilled Blind, Buried, and Through Holes on 1/2oz. Cu

<table>
<thead>
<tr>
<th>Drill &amp; Pad Diameter</th>
<th>Drill</th>
<th>Pad</th>
<th>Anti-Pad</th>
<th>PCB Thickness</th>
<th>Aspect Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IPC Class 2</strong></td>
<td>0.006&quot;</td>
<td>0.016&quot;</td>
<td>0.026&quot;</td>
<td>up to 0.039&quot;</td>
<td>6.5:1</td>
</tr>
<tr>
<td>1/2 oz copper</td>
<td>0.008&quot;</td>
<td>0.018&quot;</td>
<td>0.028&quot;</td>
<td>up to 0.062&quot;</td>
<td>7.75:1</td>
</tr>
<tr>
<td></td>
<td>0.010&quot;</td>
<td>0.020&quot;</td>
<td>0.030&quot;</td>
<td>up to 0.100&quot;</td>
<td>10.01</td>
</tr>
<tr>
<td></td>
<td>0.012&quot;</td>
<td>0.022&quot;</td>
<td>0.032&quot;</td>
<td>up to 0.120&quot;</td>
<td>10.01</td>
</tr>
<tr>
<td></td>
<td>0.0135&quot;</td>
<td>0.024&quot;</td>
<td>0.034&quot;</td>
<td>up to 0.135&quot;</td>
<td>10.01</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Drill &amp; Pad Diameter</th>
<th>Drill</th>
<th>Pad</th>
<th>Anti-Pad</th>
<th>PCB Thickness</th>
<th>Aspect Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IPC Class 3</strong></td>
<td>0.008&quot;</td>
<td>0.023&quot;</td>
<td>0.033&quot;</td>
<td>up to 0.062&quot;</td>
<td>7.75:1</td>
</tr>
<tr>
<td>1/2 oz copper</td>
<td>0.010&quot;</td>
<td>0.025&quot;</td>
<td>0.035&quot;</td>
<td>up to 0.100&quot;</td>
<td>10.01</td>
</tr>
<tr>
<td></td>
<td>0.012&quot;</td>
<td>0.027&quot;</td>
<td>0.037&quot;</td>
<td>up to 0.120&quot;</td>
<td>10.01</td>
</tr>
<tr>
<td></td>
<td>0.0135&quot;</td>
<td>0.028&quot;</td>
<td>0.038&quot;</td>
<td>up to 0.135&quot;</td>
<td>10.01</td>
</tr>
</tbody>
</table>
### Mechanical Drilled Blind, Buried, and Through Holes for Various Cu Thicknesses

<table>
<thead>
<tr>
<th>Drill &amp; Pad Diameter</th>
<th>8 Layers or less</th>
<th>&gt;8Layers</th>
<th>Drill &amp; Pad Diameter</th>
<th>8 Layers or less</th>
<th>&gt;8Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPC Class 2</td>
<td>Pad dia over drill</td>
<td>Pad dia over drill</td>
<td>IPC Class 3A</td>
<td>Pad dia over drill</td>
<td>Pad dia over drill</td>
</tr>
<tr>
<td>1/4 oz copper</td>
<td>0.010&quot;</td>
<td>0.010&quot;</td>
<td>1/2 oz copper</td>
<td>0.015&quot;</td>
<td>0.015&quot;</td>
</tr>
<tr>
<td>3/8 oz copper</td>
<td>0.010&quot;</td>
<td>0.010&quot;</td>
<td>1 oz copper</td>
<td>0.017&quot;</td>
<td>0.017&quot;</td>
</tr>
<tr>
<td>1/2 oz copper</td>
<td>0.010&quot;</td>
<td>0.010&quot;</td>
<td>2 oz copper</td>
<td>0.018&quot;</td>
<td>0.018&quot;</td>
</tr>
<tr>
<td>1 oz copper</td>
<td>0.012&quot;</td>
<td>0.012&quot;</td>
<td>2 oz copper</td>
<td>0.018&quot;</td>
<td>0.018&quot;</td>
</tr>
<tr>
<td>2 oz copper</td>
<td>0.014&quot;</td>
<td>0.014&quot;</td>
<td>1 oz copper</td>
<td>0.015&quot;</td>
<td>0.015&quot;</td>
</tr>
<tr>
<td>3 oz copper</td>
<td>0.016&quot;</td>
<td>0.016&quot;</td>
<td>1/2 oz copper</td>
<td>0.013&quot;</td>
<td>0.015&quot;</td>
</tr>
<tr>
<td>4 oz copper</td>
<td>0.018&quot;</td>
<td>0.018&quot;</td>
<td>1 oz copper</td>
<td>0.017&quot;</td>
<td>0.017&quot;</td>
</tr>
</tbody>
</table>

### DFM Guidelines: Annular Ring Requirements For IPC Classes II & III

22
Electrolytic copper is plated in the hole barrel to its final thickness.

Electrolytic copper is plated on top of the base copper foil and electroless copper.
DFM Guidelines: Outer Layers and Subs Have Added Cu Plating
DFM Guidelines: VIPPO adds extra Cu plating before etch

- Background copper composed of copper foil with a electrolytic copper plating and Electroless Cu
- Pattern plated circuit image building
  Up additional copper thickness

Step 13: Strip photo resist leaving exposed background copper
  with pattern plated copper image protected with a tin lead resist
DFM Guidelines: Etched Lines/spaces increase with Cu weight

Difficulties with heavier Cu designs using 0.5mm pitch QFNs
# Standard PCB Design Guidelines - Green is Good

## Trace & Space

<table>
<thead>
<tr>
<th>Feature</th>
<th>Standard</th>
<th>Advanced</th>
<th>Engineering</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Trace</td>
<td>0.004&quot; - 100 μm</td>
<td>0.003&quot; - 75 μm</td>
<td>0.002&quot; - 50 μm</td>
<td>0.0018&quot; - 40 μm</td>
</tr>
<tr>
<td>Internal Trace</td>
<td>0.004&quot; - 100 μm</td>
<td>0.003&quot; - 75 μm</td>
<td>0.002&quot; - 50 μm</td>
<td>0.0018&quot; - 40 μm</td>
</tr>
<tr>
<td>Internal Space</td>
<td>0.004&quot; - 100 μm</td>
<td>0.003&quot; - 75 μm</td>
<td>0.002&quot; - 50 μm</td>
<td>0.0018&quot; - 40 μm</td>
</tr>
</tbody>
</table>

## Drilled Via Size

<table>
<thead>
<tr>
<th>Feature</th>
<th>Standard</th>
<th>Advanced</th>
<th>Engineering</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drill Diameter</td>
<td>0.010&quot; - 254 μm</td>
<td>0.008&quot; - 200 μm</td>
<td>0.006&quot; - 150 μm</td>
<td>0.004&quot; - 100 μm</td>
</tr>
<tr>
<td>Pad Diameter</td>
<td>0.020&quot; - 508 μm</td>
<td>0.016&quot; - 400 μm</td>
<td>0.012&quot; - 300 μm</td>
<td>0.004&quot; - 100 μm</td>
</tr>
</tbody>
</table>

## Aspect Ratio

<table>
<thead>
<tr>
<th>Drill Diameter</th>
<th>Standard</th>
<th>Advanced</th>
<th>Engineering</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.006&quot; - 150 μm drill</td>
<td>8:1</td>
<td>6.5:1</td>
<td>10:1</td>
<td>14:1</td>
</tr>
<tr>
<td>0.008&quot; - 200 μm drill</td>
<td>10:1</td>
<td>10:1</td>
<td>12:1</td>
<td>16:1</td>
</tr>
<tr>
<td>0.010&quot; - 254 μm drill</td>
<td>10:1</td>
<td>12:1</td>
<td>16:1</td>
<td>18:1</td>
</tr>
<tr>
<td>0.012&quot; - 300 μm drill</td>
<td>10:1</td>
<td>14:1</td>
<td>18:1</td>
<td>20:1</td>
</tr>
<tr>
<td>0.013.5&quot; - 342 μm drill</td>
<td>10:1</td>
<td>16:1</td>
<td>20:1</td>
<td>24:1</td>
</tr>
</tbody>
</table>

## Microvia

<table>
<thead>
<tr>
<th>Feature</th>
<th>Standard</th>
<th>Advanced</th>
<th>Engineering</th>
<th>Development</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via Diameter</td>
<td>150 μm &amp; 125 μm</td>
<td>0.004&quot; - 100 μm</td>
<td>0.006&quot; - 150 μm</td>
<td>0.004&quot; - 100 μm</td>
</tr>
<tr>
<td>Pad Diameter</td>
<td>300 μm &amp; 254 μm</td>
<td>0.008&quot; - 200 μm</td>
<td>0.010&quot; - 254 μm</td>
<td>0.007&quot; - 175 μm</td>
</tr>
<tr>
<td>Aspect Ratio</td>
<td>0.6:1</td>
<td>0.8:1</td>
<td>1:1</td>
<td>1:1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Year</th>
<th>2015</th>
<th>2015</th>
<th>2015</th>
<th>2016</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
# Standard PCB Design Guidelines

<table>
<thead>
<tr>
<th>Feature</th>
<th>Standard</th>
<th>Advanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drill-to-Copper</td>
<td>0.008&quot;</td>
<td>0.0065&quot;</td>
</tr>
<tr>
<td>Anti-Pad</td>
<td>0.010&quot; over Pad dia</td>
<td>0.008&quot; over Pad dia</td>
</tr>
<tr>
<td>Thermal Relief</td>
<td></td>
<td></td>
</tr>
<tr>
<td>non Plated Layer</td>
<td>0.006&quot;/side</td>
<td>0.004&quot;/side</td>
</tr>
<tr>
<td>Plated Layer</td>
<td>0.008&quot;/side</td>
<td>0.006&quot;/side</td>
</tr>
<tr>
<td>Circuit to PCB edge</td>
<td>0.025&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td>Plane to PCB edge</td>
<td>0.025&quot;</td>
<td>0.010&quot;</td>
</tr>
<tr>
<td>Routing Tolerance</td>
<td>+/- 0.005&quot;</td>
<td>+/- 0.002&quot;</td>
</tr>
<tr>
<td>Edge of hole barrel to PCB Edge</td>
<td>0.025&quot;</td>
<td>0.020&quot;</td>
</tr>
<tr>
<td>Solder Mask Dam</td>
<td>0.004&quot; min</td>
<td>0.003&quot; min</td>
</tr>
<tr>
<td>Filled Vias</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Conductive</td>
<td>0.012&quot; drill min</td>
<td>0.010&quot; drill min</td>
</tr>
<tr>
<td>non-conductive</td>
<td>0.010&quot; drill min</td>
<td>0.008&quot; drill min</td>
</tr>
</tbody>
</table>

*Via-in-Pad filled & plated over require wrap around plating. Wrap around plating reduces trace & space capabilities on plated layers.*
### Stack-up Design Example: 0.65mm BGA Class 3 w/High Voltage

#### Design Constraints:
- High Volume, Class 3 for Asia
- .65mm (25.6mil) pitch (but high reliability – use uvias)
- Lowest cost – L1-L3 skip via (13/23mil drill/pad)
- Controlled impedances
- High V L1-L4 thickness>16mil anti-CAF (added later)

#### Design Details:

**Materials:** Isola 370H High Tg FR4

**Layers and Specifications:**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Calc Thickness</th>
<th>Description</th>
<th>Dk / Df</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.0021</td>
<td>1oz P/G</td>
<td>3.91 / 0.0210</td>
</tr>
<tr>
<td>2</td>
<td>0.0030</td>
<td>370H</td>
<td>3.01 / 0.0210</td>
</tr>
<tr>
<td>3</td>
<td>0.0030</td>
<td>1/2oz Sg</td>
<td>4.25 / 0.0190</td>
</tr>
<tr>
<td>4</td>
<td>0.0012</td>
<td>370H</td>
<td>3.01 / 0.0210</td>
</tr>
<tr>
<td>5</td>
<td>0.0012</td>
<td>1oz P/G</td>
<td>3.91 / 0.0210</td>
</tr>
<tr>
<td>6</td>
<td>0.0012</td>
<td>0.0090 (10-20mil)</td>
<td>3.01 / 0.0210</td>
</tr>
<tr>
<td>7</td>
<td>0.0012</td>
<td>1/2oz Sg</td>
<td>4.25 / 0.0190</td>
</tr>
<tr>
<td>8</td>
<td>0.0012</td>
<td>370H</td>
<td>3.01 / 0.0210</td>
</tr>
</tbody>
</table>

**Impedance Matrix:**

<table>
<thead>
<tr>
<th>Impedance Type</th>
<th>Layer</th>
<th>Design</th>
<th>Actual</th>
<th>Pitch</th>
<th>Plane</th>
<th>Target</th>
<th>Tol (ohms)</th>
<th>Predict</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stripline</td>
<td>L3</td>
<td>-</td>
<td>0.00575</td>
<td>-</td>
<td>L2</td>
<td>40</td>
<td>4.0</td>
<td>40.06</td>
</tr>
<tr>
<td>Stripline</td>
<td>L3</td>
<td>-</td>
<td>0.00375</td>
<td>-</td>
<td>L2</td>
<td>50</td>
<td>5.0</td>
<td>50.06</td>
</tr>
<tr>
<td>EC Stripline</td>
<td>L3</td>
<td>0.0040</td>
<td>0.0045</td>
<td>0.0085</td>
<td>L2</td>
<td>80</td>
<td>8.0</td>
<td>79.80</td>
</tr>
<tr>
<td>EC Stripline</td>
<td>L3</td>
<td>-</td>
<td>0.0035</td>
<td>0.0140</td>
<td>L2</td>
<td>100</td>
<td>10.0</td>
<td>100.51</td>
</tr>
<tr>
<td>Stripline</td>
<td>L5</td>
<td>-</td>
<td>0.00575</td>
<td>-</td>
<td>L5</td>
<td>40</td>
<td>4.0</td>
<td>40.06</td>
</tr>
<tr>
<td>Stripline</td>
<td>L6</td>
<td>-</td>
<td>0.00375</td>
<td>-</td>
<td>L5</td>
<td>50</td>
<td>5.0</td>
<td>50.06</td>
</tr>
<tr>
<td>Stripline</td>
<td>L5</td>
<td>-</td>
<td>0.0040</td>
<td>0.0045</td>
<td>L5</td>
<td>80</td>
<td>8.0</td>
<td>79.80</td>
</tr>
<tr>
<td>EC Stripline</td>
<td>L6</td>
<td>-</td>
<td>0.0035</td>
<td>0.0140</td>
<td>L5</td>
<td>100</td>
<td>10.0</td>
<td>100.51</td>
</tr>
</tbody>
</table>

**Impedance Requirements:**

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Req. Thickness</th>
<th>Tol +</th>
<th>Tol -</th>
<th>Calc Thick</th>
</tr>
</thead>
<tbody>
<tr>
<td>Incl. Pating Mask</td>
<td>0.0620</td>
<td>0.0062</td>
<td>0.0062</td>
<td>0.0616</td>
</tr>
<tr>
<td>Incl. Mask over Laminate</td>
<td>0.0566</td>
<td>0.0058</td>
<td>0.0058</td>
<td>0.0562</td>
</tr>
<tr>
<td>Incl. Pating</td>
<td>0.0610</td>
<td>0.0061</td>
<td>0.0061</td>
<td>0.0606</td>
</tr>
<tr>
<td>After Lamination</td>
<td>0.0562</td>
<td>0.0029</td>
<td>0.0029</td>
<td>0.0573</td>
</tr>
<tr>
<td>Over Laminate</td>
<td>0.0270</td>
<td>0.0008</td>
<td>0.0008</td>
<td>0.0272</td>
</tr>
</tbody>
</table>
Stack-up Design Example: 0.65mm BGA Class 3 w/High Voltage (Interim Version)

Design Constraints:
- High Volume, Class 3 for Asia
- .65mm pitch (23mil pads were too large)
- Added lamination cycle – cost
- Added buried via – cost
- fill – cost
- Controlled impedance linewidths min 4mil
- High V L1-L4 thickness>16mil anti-CAF

**Impedance Table**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Structure Type</th>
<th>Coated Microstrip</th>
<th>Target Impedance (ohms)</th>
<th>Impedance Tolerance (ohms)</th>
<th>Target Line Width (mil)</th>
<th>Differential Spacing (mil)</th>
<th>Referenced Layers</th>
<th>Modelled Linewidth (mil)</th>
<th>Modelled Spacing (mil)</th>
<th>Modelled Impedance (ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Single Ended</td>
<td>Yes</td>
<td>46.00</td>
<td>+/-4</td>
<td>4.00</td>
<td>(2)</td>
<td>7.20</td>
<td>40.27</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>1</td>
<td>Single Ended</td>
<td>Yes</td>
<td>56.00</td>
<td>+/-5</td>
<td>4.00</td>
<td>(2)</td>
<td>6.00</td>
<td>40.13</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>1</td>
<td>Edge Coupled</td>
<td>Yes</td>
<td>80.00</td>
<td>+/-6</td>
<td>5.00</td>
<td>(2)</td>
<td>8.00</td>
<td>40.15</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>1</td>
<td>Edge Coupled</td>
<td>Yes</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.00</td>
<td>(2)</td>
<td>10.00</td>
<td>90.83</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>3</td>
<td>Single Ended</td>
<td>No</td>
<td>46.00</td>
<td>+/-4</td>
<td>4.00</td>
<td>(4)</td>
<td>6.00</td>
<td>40.13</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>3</td>
<td>Single Ended</td>
<td>No</td>
<td>56.00</td>
<td>+/-5</td>
<td>4.00</td>
<td>(4)</td>
<td>6.00</td>
<td>40.13</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>3</td>
<td>Edge Coupled</td>
<td>No</td>
<td>80.00</td>
<td>+/-6</td>
<td>4.00</td>
<td>(4)</td>
<td>4.40</td>
<td>40.15</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>3</td>
<td>Edge Coupled</td>
<td>No</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.00</td>
<td>(4)</td>
<td>10.00</td>
<td>90.83</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>6</td>
<td>Single Ended</td>
<td>No</td>
<td>46.00</td>
<td>+/-4</td>
<td>4.00</td>
<td>(6)</td>
<td>5.00</td>
<td>40.13</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>6</td>
<td>Single Ended</td>
<td>No</td>
<td>56.00</td>
<td>+/-5</td>
<td>4.00</td>
<td>(6)</td>
<td>5.00</td>
<td>40.13</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>6</td>
<td>Edge Coupled</td>
<td>No</td>
<td>80.00</td>
<td>+/-6</td>
<td>4.00</td>
<td>(6)</td>
<td>4.40</td>
<td>40.15</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>6</td>
<td>Edge Coupled</td>
<td>No</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.00</td>
<td>(6)</td>
<td>10.00</td>
<td>90.83</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>8</td>
<td>Single Ended</td>
<td>No</td>
<td>46.00</td>
<td>+/-4</td>
<td>4.00</td>
<td>(7)</td>
<td>7.20</td>
<td>40.27</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>8</td>
<td>Single Ended</td>
<td>No</td>
<td>66.00</td>
<td>+/-6</td>
<td>4.00</td>
<td>(7)</td>
<td>4.60</td>
<td>40.27</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>8</td>
<td>Edge Coupled</td>
<td>No</td>
<td>80.00</td>
<td>+/-6</td>
<td>4.00</td>
<td>(7)</td>
<td>4.80</td>
<td>40.27</td>
<td></td>
<td>50.13</td>
</tr>
<tr>
<td>8</td>
<td>Edge Coupled</td>
<td>Yes</td>
<td>100.00</td>
<td>+/-10</td>
<td>4.00</td>
<td>(7)</td>
<td>4.00</td>
<td>10.00</td>
<td></td>
<td>90.83</td>
</tr>
</tbody>
</table>

**Drill Table**

<table>
<thead>
<tr>
<th>Start Layer</th>
<th>End Layer</th>
<th>Drill Type</th>
<th>Plate Type</th>
<th>Via Fill</th>
<th>Drill Size [mm]</th>
<th>Drill Depth</th>
<th>Pad Size [mil]</th>
<th>Stacked Vias</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8</td>
<td>Mech</td>
<td>PTH &amp; MPT</td>
<td></td>
<td>6.00</td>
<td>21.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>7</td>
<td>Mech</td>
<td>Buried Via</td>
<td>Non-Conductive Via Fill (Flat)</td>
<td>6.00</td>
<td>19.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>Laser</td>
<td>Micro Via</td>
<td></td>
<td>4.00</td>
<td>12.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>Laser</td>
<td>Micro Via</td>
<td>Non-Conductive Via Fill (Flat)</td>
<td>4.50</td>
<td>12.50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>7</td>
<td>Laser</td>
<td>Micro Via</td>
<td></td>
<td>4.00</td>
<td>12.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>Laser</td>
<td>Micro Via</td>
<td>Non-Conductive Via Fill (Flat)</td>
<td>4.50</td>
<td>12.50</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Files Required for PCB Fabrication

Required:
1. Gerber Files (RS-274-X or RS-274-D format)
   - All copper layers (including inner and outer layers)
   - Solder mask layers
   - Silkscreen/Legend layers
   - Via plugging layers (if applicable)
   - Solder paste layers (for board assembly)
   - Aperture list if apertures are not embedded in the Gerber data (i.e. not using RS-274-X)
2. Drill file with tool codes and X-Y coordinates for all holes (ASCII or EIA format).
3. IPC-D-356 netlist (used for continuity testing).
4. Readme File containing Engineering contact information and any special instructions.
5. Fab drawing
   - Board outline, dimensions, including cutouts, chamfers, radii, bevels, scores, etc.
   - Dimensions from a reference hole in the board to a corner or to two sides of the board outline.
   - A drill chart with the hole symbols on the drawing and the finished hole sizes
   - Material requirements
   - Finished board thickness and tolerance
   - Layer stack-up order
   - Controlled impedance requirements (if applicable)
   - Dimensioned array drawing if the design is to be shipped as a multiple-up array
   - Notes defining any other requirements or specifications pertinent to the design

Optional:
1. Valor ODB++ file - preferred by PCB vendors instead of Gerber format.
2. Check plots in Adobe PDF form. Incoming QC uses this to check PCB.
Downstream Victims of Incomplete or Missing Fab Drawing

* Users – technical or non-technical - who have to review a Fab Drawing to do their job
** Users who print a copy of the Fab Drawing to do their job, because they don’t have a gerber viewer and/or they can’t see the full drawing on a monitor

- PCB Sales & Customer support
  - Field sales
  - FAEs*
  - Inside customer service reps*
  - Customer service managers*
  - Estimators*
  - Site Applications Engineers*

- Assemblers & Contract Manufacturers
  - Field sales
  - Quote team*
  - Process Engineers*
  - Program managers
  - Commodity managers
  - Buyers*
  - Receiving Inspectors***
  - Quality engineers

- PCB Fabricators After Receipt of Order (ARO)
  - Inside customer service reps
  - Stack-up techs*
  - Front-end engineer manager
  - Planners***
  - CAM technicians***
  - Process engineers
  - Routing operators***
  - QC Inspectors***
Assembler to Fabricator Communication Flow Diagram
Elements Required in a PCB Fabrication Drawing

- Title Block with Part Number and Rev
- Fabrication Notes
- Mechanical drawing with dimensions
  - Single unit
    - With or without rails
  - Multiple-up array with rails for assembly
    - Includes arrays designed with required spacing for testing
- Layer construction (stack-up)
  - Material type
  - Overall thickness
  - Layer copper thicknesses
  - Special dielectric thicknesses, if required
  - Controlled impedance, if required
- Drill Table (including through, blind, buried, microvia, and back-drill holes)
AFTER FINAL PLATING, PLANARIZE THE HIGH POWER PADS ON BOTH SIDES
WITH A SURFACE FINISH OF 63 MICROINCHES AND .005 TIR MAX. THE
EDGES OF THE HIGH POWER PADS AND TRACES SHALL BE SMOOTH AND FREE OF SHARP EDGES.

HOLES SIZES: ARE AFTER METALIZED PLATING.
HOLES LOCATION: TOLERANCE: SHALL BE DRILLED WITHIN .001" DIAMETER OF PAD CENTER.
BARREL PLATING: THROUGH HOLES TO BE .8 MIL MIN. THICK COPPER.

- 1oz Copper
- No Silk Screen
- Gold Everywhere
- NO Hole Plating Anywhere (all sizes are finish diameter)

ALL PLATED THROUGH HOLES TO HAVE A MINIMUM OF .001" COPPER.
5- APPLY SOLDERMASK (LIQUID PHOTO IMAGABLE) OVER BARE COPPER, SOLDER
BE PER IPC-SM-844, TYPE B, CLASS 2, COLOR: TRANSPARENT BLACK.
6- FINISH SHALL BE IMMERSION GOLD.

CLEARANCE FROM EXISTING COPPER AND SHOULD NOT BE PLACED UNDER SURFACE MOUNT DEVICES

8.) CLEANLINESS & PACKAGING: BOARDS ARE TO BE FREE OF NOTICABLE COSMETIC FLAWS.

FINISH: GOLD PLATE OUTER MOST LAYERS, >99.5% PURITY, 200 ± 25 NANOMETER THICK.

15. VENDOR MUST RUN AUTOSILK TO BREAK SILKSCREEN FROM VIAS AND PADS

<table>
<thead>
<tr>
<th>Boardside Coupled</th>
</tr>
</thead>
<tbody>
<tr>
<td>98.5</td>
</tr>
</tbody>
</table>

20. REMOVE SILKSCREEN FROM SOLDERABLE SURFACES. DO NOT CLIP BUT REMOVE THE ILLEGAL LEGENDS.

Layer2 is GND plane.

17. INCLUDE 3 GLOBE TOOLING HOLE UNPLATED