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AltiumLive 2017:
Adopting Early Analysis of Your Power Delivery Network

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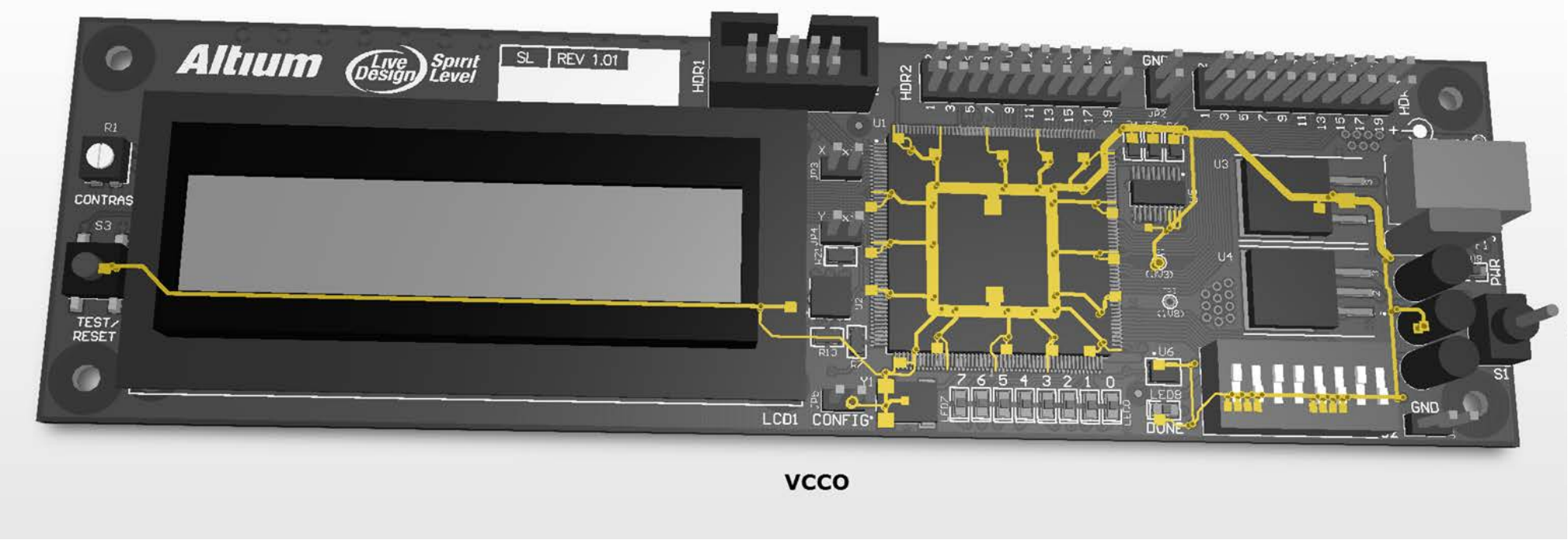
What is a PDN?

PDN is an acronym for “Power Delivery Network”

A PDN is the collection of all power specific components, traces, planes, and interconnects



Also referred to as a “Power Distribution Network”

Why Power Integrity has become such a concern

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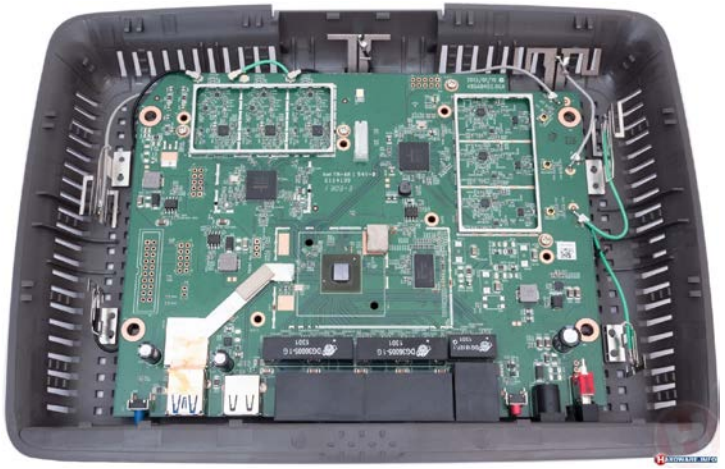
High density, high speed, or high power designs have challenging power requirements

High Density



High Speed

High Current

Getting power delivery right is critical for all types of today's system designs

Common Symptoms of Power Related Problems

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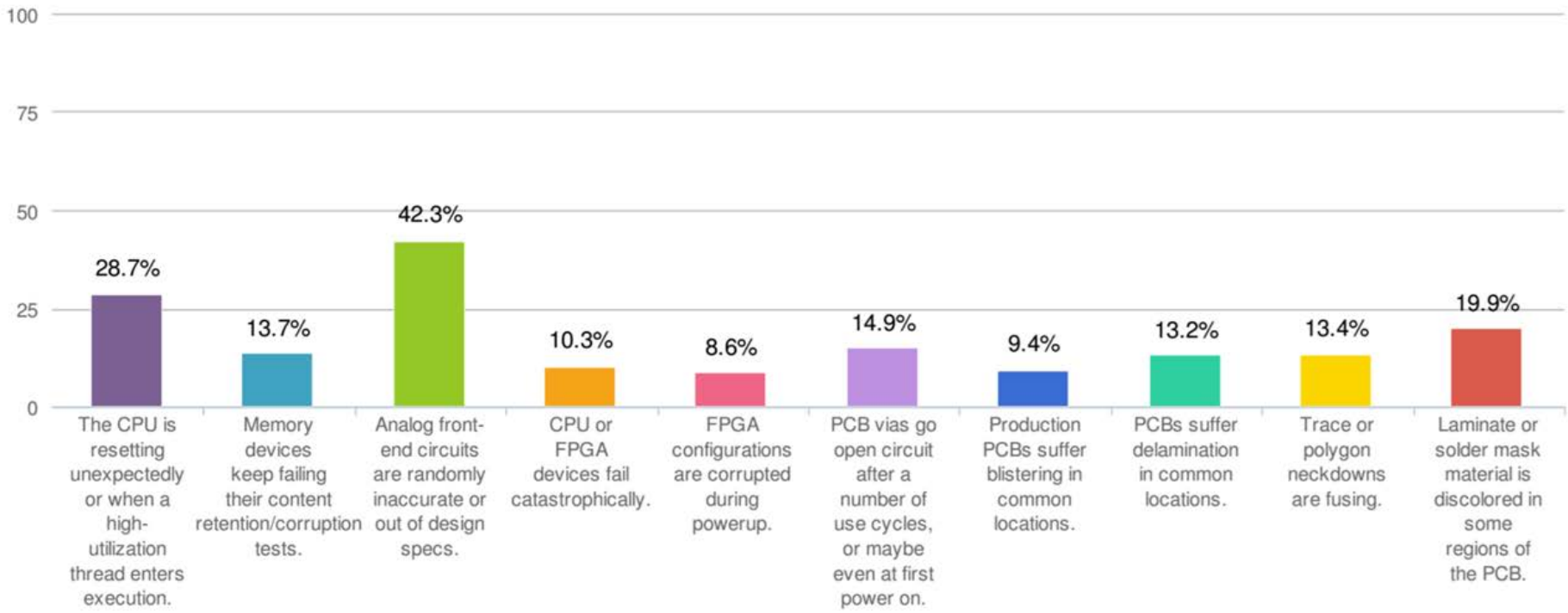
A poorly designed PDN can be the root cause of many difficult-to-diagnose problems



PDN Problems Reported by Surveyed Users

A well designed PDN is essential for optimal product cost, performance and reliability

My boards work fine, why use PDN Analysis?

A board may not perform well under all required conditions

- Marginal power routing is subject to

  Increased temperature → higher resistivity and component behavior changes

  Component tolerance and process variation

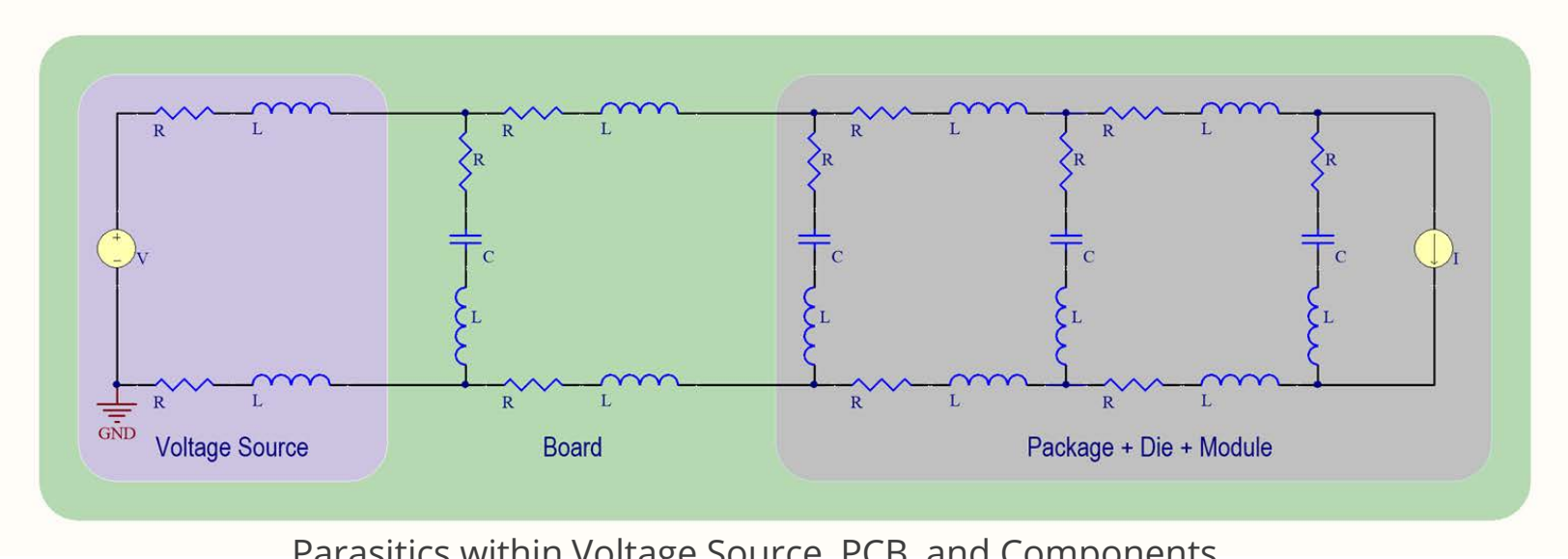
- The PDN should be verified under worst case conditions
- PDN problems are easiest to address during the design phase

"As engineers we don't always recognize the simple things - we often miss the forest for the trees. Because of PDNA, in one design just by moving vias I increased the performance and lowered the current density a full factor - 48 mA per mil sq to 22 mA per mil sq"
Tim Tabor, Tabor Engineering

AC Parasitics

Noise on power and return rails

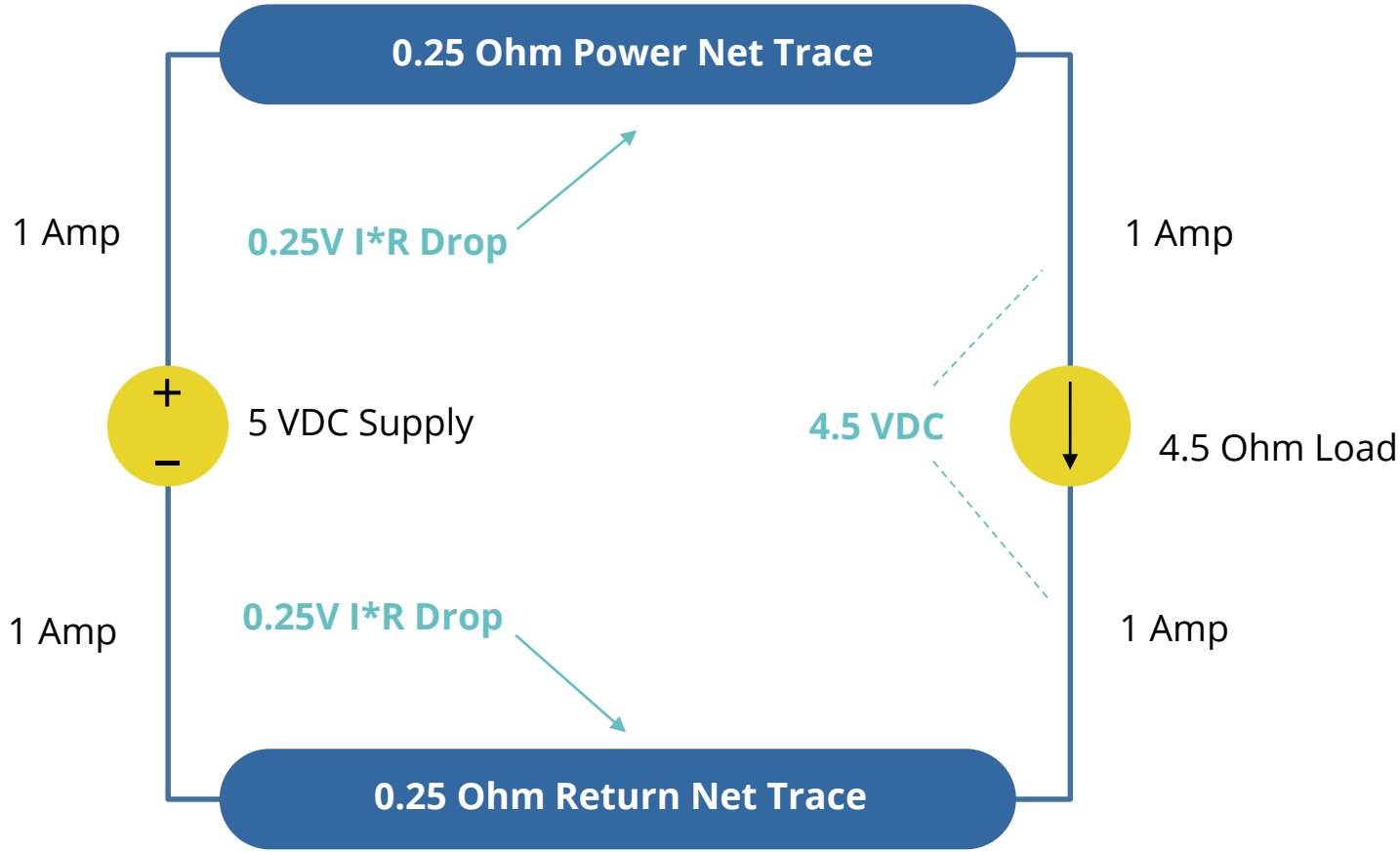
- Noise is proportional to the network's impedance and the transient current draw
- Noise on power rails can adversely impact *signal* integrity



Parasitics within Voltage Source, PCB, and Components

A PDN by definition includes all resistive, inductive, and capacitive parasitics

The Relationship between Voltage, Current, and Resistance

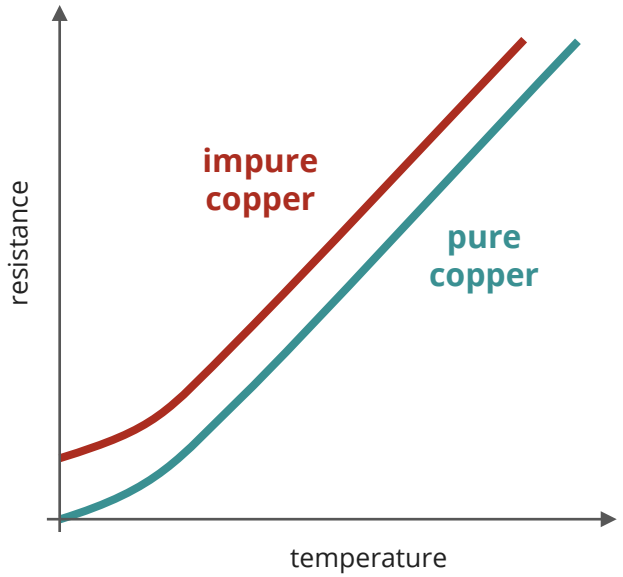


Voltage Drop = Current x Resistance

Less than 1 Ohm of resistance can significantly impact voltage level at the load

PCB copper conductivity can vary

Fabricated PCB copper is less conductive than pure copper

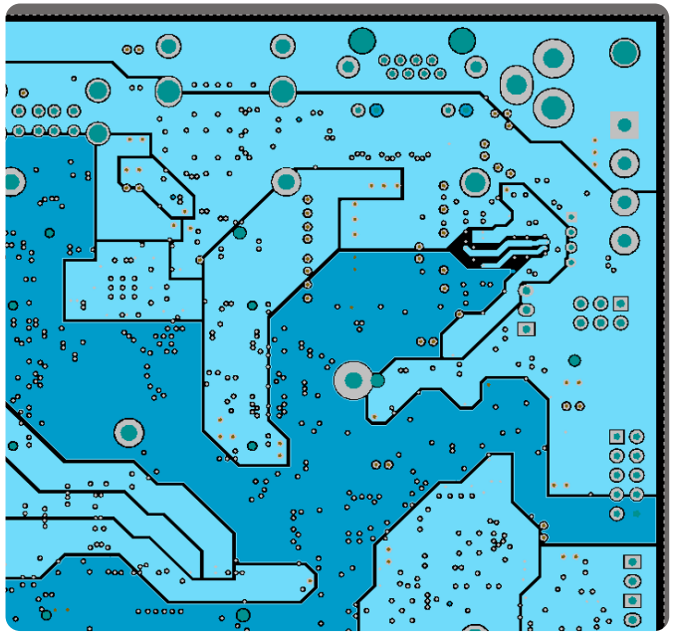


PCB Copper Resistance Relative to Temperature

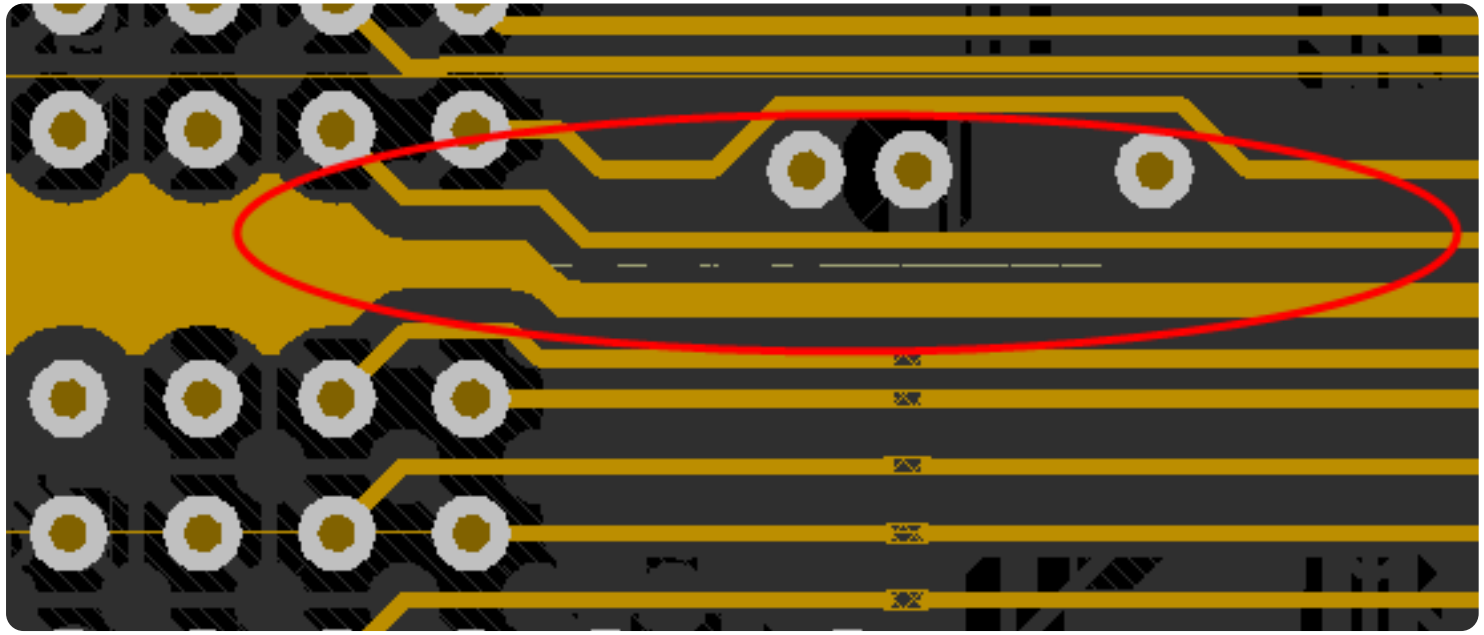
The resistivity of PCB copper varies with temperature

Voltage Drops

Resistance between the power source and load results in a lower voltage at the load



Lengthy meandering power plane splits



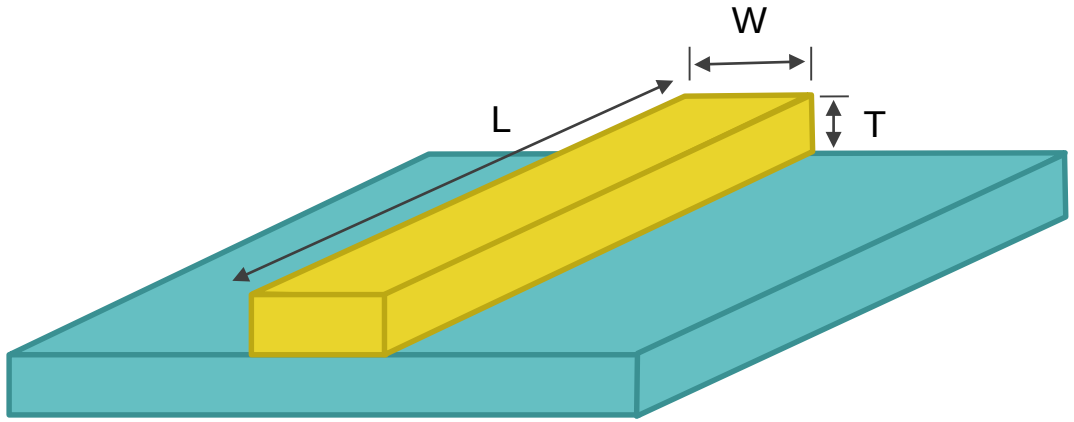
Power polygon compromised by vias and tracks

Reduced voltage at loads can lead to intermittent functional problems

The Relationship between Area, Current Density, and Heat

Current density is the current per unit area of cross sectional copper

- As cross sectional area (W*T) decreases, current density increases
- Increased current density means more voltage drop per unit length (L)
- Increased current density also results in higher copper temperature

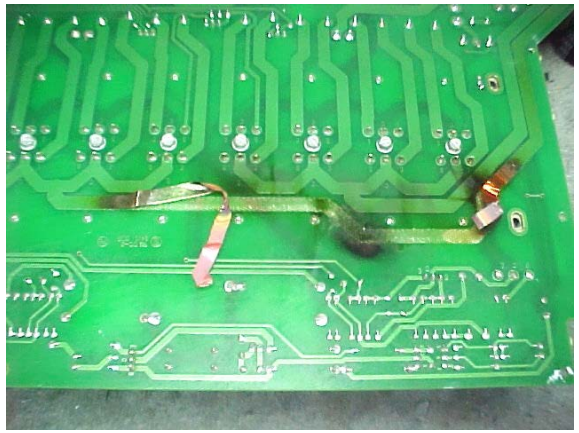


Copper Conductor Dimensions

Current density is a key factor in PDN quality

High Current Density

An inadequate amount of copper to conduct current results in high current density



Inadequate copper can fuse open

High current can melt Via plating

Heat can warp or delaminate the board

Heat can damage the physical PCB and shorten component life span

And what about too much copper?

Excess copper consumes valuable board space

Can power requirements still be safely met after *reducing* copper?

Critical for achieving an optimal PDN layout given limited board space

Space and Area Constrained Wearable Product PCB

Board space is heavily constrained for wearable and other high density products

How does the Designer Verify PDN?

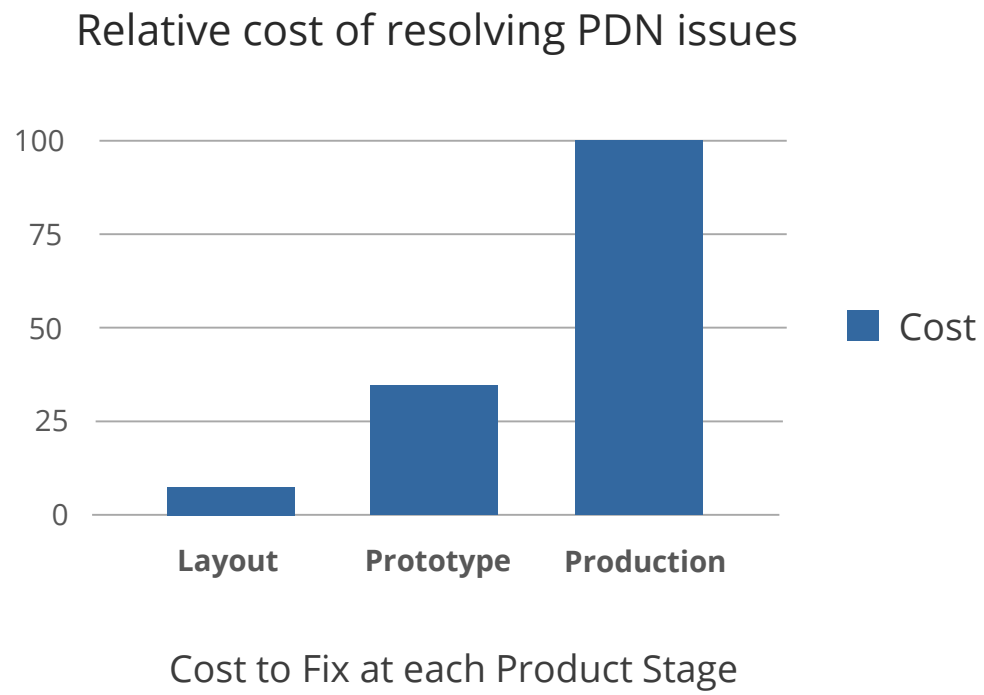
Need to verify Voltage Drops and Current Density between Sources and Loads

- **Wait for first prototype**

  Measure actual results
  Reactive, costly

- **Iteratively simulate during layout**

  Explore options and corner cases
  Proactive, faster, lower cost



It is essential that PDN issues are identified and resolved early during layout

Integrating PDN Analysis into your Design Methodology

Prior to any fabrication, a PDN Analysis methodology can:

- Provide early insight into PDN problems
- Enable the designer to explore various PDN layout alternatives
- Provide a means to test corner case conditions
- Improve reliability by intelligently determining the distribution of copper
- Reduce product cost by reducing layer count

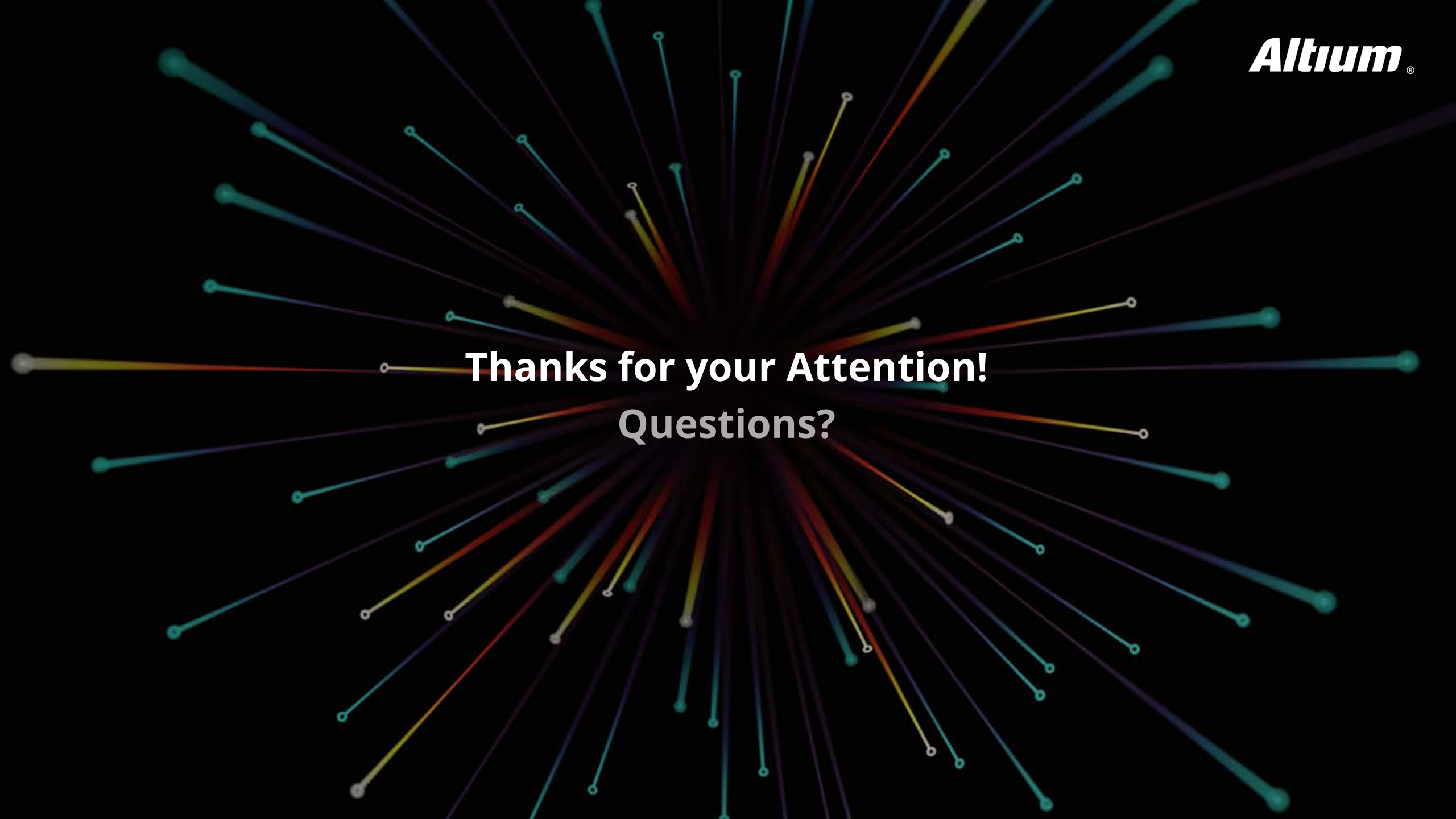
Ensure higher quality PDN design by adopting a PDN analysis methodology

Best Practices to Avoid PDN Problems

Adopt a static solver based PDN analysis methodology

- Don’t wait until first prototype to verify PDN in the lab
- Resolve marginal voltage levels at critical devices
- Carefully inspect any objects of highest simulated current density
- Ensure that all copper can handle the worst-case loading conditions
- Analyze early and often during layout

It is easier and less costly to visualize and resolve problems during layout than in hardware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Thanks for your Attention!
Questions?